

**IT8761E**

***Legacy Low Pin Count I/O***

***(Code Name: Humming Bird)***

**Preliminary Specification V0.3**

Copyright © 2000 ITE, Inc.

This is Preliminary document release. All specifications are subject to change without notice.  
The material contained in this document supersedes all previous documentation issued for the related products included herein. Please contact ITE, Inc. for the latest document(s).

All sales are subject to ITE's Standard Terms and Conditions, a copy of which is included in the back of this document.

ITE and IT8761E are trademarks of ITE, Inc.  
Intel, LPC are claimed as trademarks by Intel Corp.  
Microsoft is claimed as a trademark by Microsoft Corporation.  
PCI™ is a registered trademark of PCI Special Interest Group.  
All trademarks are the properties of their respective owners.  
All specifications are subject to change without notice.

Additional copies of this manual or other ITE literature may be obtained from:

ITE (USA) Inc.	<b>Phone:</b> (408) 530-8860
Marketing Department	<b>Fax:</b> (408) 530-8861
1235 Midas Way	
Sunnyvale, CA 94086	
U.S.A.	

ITE (USA) Inc.	<b>Phone:</b> (512) 388-7880
Eastern U.S.A. Sales Office	<b>Fax:</b> (512) 388-3108
896 Summit St., #105	
Round Rock, TX 78664	
U.S.A.	

ITE, Inc.	<b>Phone:</b> (02) 2657-9896
Marketing Department	<b>Fax:</b> (02) 2657-8561, 2657-8576
7F, No. 435, Nei Hu District, Jui Kuang Road,	
Taipei 114, Taiwan, R.O.C.	

If you have any marketing or sales questions, please contact:

**Lawrence Liu**, at ITE Taiwan: E-mail: [lawrence.liu@ite.com.tw](mailto:lawrence.liu@ite.com.tw), Tel: 886-2-26579896 X6071,  
Fax: 886-2-26578561

**David Lin**, at ITE U.S.A: E-mail: [david.lin@iteusa.com](mailto:david.lin@iteusa.com), Tel: (408) 980-8168 X238,  
Fax: (408) 980-9232

**Don Gardenhire**, at ITE Eastern USA Office: E-mail: [don.gardenhire@iteusa.com](mailto:don.gardenhire@iteusa.com),  
Tel: (512) 388-7880, Fax: (512) 388-3108

To find out more about ITE, visit our World Wide Web at:

<http://www.iteusa.com>

<http://www.ite.com.tw>

Or e-mail [itesupport@ite.com.tw](mailto:itesupport@ite.com.tw) for more product information/services.

### Revision History

Section	Revision	Page No.
1	• In the features of Keyboard Controller, the 5 <sup>th</sup> feature item in the previous version was removed.	1-1
6	• In section 6.3.2.5 KBC Special Configuration Register, the bits 7-5 were revised to "Reserved".	6-11

## CONTENTS

Page

<b>1. Features .....</b>	<b>1-1</b>
<b>2. General Description.....</b>	<b>1-1</b>
<b>3. Pin Configuration .....</b>	<b>3-1</b>
<b>4. Pin Description .....</b>	<b>4-1</b>
<b>5. Functional Description.....</b>	<b>5-1</b>
5.1 Reset Strapping Options.....	5-1
5.2 LPC Interface .....	5-1
5.2.1 Overview .....	5-1
5.2.2 LPC Transactions .....	5-1
5.2.3 LPC I/F Block Diagram .....	5-2
5.3 GPIO.....	5-3
5.4 Testability.....	5-4
<b>6. Register Description.....</b>	<b>6-1</b>
6.1 Standard ISA Plug-and-Play (PnP) High Level Register Map.....	6-1
6.2 Global Configuration Register Set Description.....	6-4
6.3 PnP Configuration Registers Description .....	6-6
6.3.1 IT8761E Global PnP Registers .....	6-6
6.3.1.1 Configure Control Register .....	6-6
6.3.1.2 Logical Device Number Register.....	6-6
6.3.1.3 Chip ID Number Register .....	6-6
6.3.1.4 Chip Version Number Register .....	6-7
6.3.1.5 LPC to X-bus PIO Timing Register .....	6-7
6.3.1.6 LPC to X-bus DMA Timing Register.....	6-7
6.3.1.7 Chip Test Mode Enable Register .....	6-8
6.3.1.8 Other registers not listed above with index between 00h~2Fh .....	6-8
6.3.2 IT8761E KBC PnP Registers (LDN=00h) .....	6-9
6.3.2.1 KBC Function Enable Control Register .....	6-9
6.3.2.2 KBC Module Base Address Registers .....	6-9
6.3.2.3 KBC Interrupt Control Register .....	6-10
6.3.2.4 KBC Interrupt Type Register.....	6-10
6.3.2.5 KBC Special Configuration Register .....	6-11
6.3.2.6 Emulated KBC Host Interface Control Register.....	6-12
6.3.3 IT8761E UART PnP Registers (LDN=01h) .....	6-13
6.3.3.1 UART Module Base Address Registers.....	6-13
6.3.3.2 UART Interrupt Control Register.....	6-13
6.3.3.3 UART Interrupt Type Register .....	6-14
6.3.3.4 UART Special Configuration Register .....	6-14
6.3.4 IT8761E GPIO PnP Registers (LDN=02h).....	6-15
6.3.4.1 GPIO Module Base Address Registers .....	6-15
6.3.4.2 GPIO Interrupt Control Register .....	6-15
6.3.4.3 GPIO Interrupt Type Register .....	6-16

6.3.4.4	GPIO Input / Output Selection Registers .....	6-16
6.3.4.5	GPIO Input Interrupt Mask Registers .....	6-17
6.3.4.6	GPIO Interrupt Trigger Edge Registers .....	6-17
6.3.4.7	GPIO De-bounce Register .....	6-18
6.3.4.8	GPIO Blinking Register .....	6-18
6.3.4.9	Software Interrupt Registers .....	6-19
6.3.4.10	GPIO Special Configuration Register .....	6-21
6.3.5	IT8761E FDC PnP Registers (LDN=03h) .....	6-22
6.3.5.1	FDC Function Enable Control Register .....	6-22
6.3.5.2	FDC Module Base Address Registers .....	6-22
6.3.5.3	FDC Interrupt Control Register .....	6-22
6.3.5.4	FDC Interrupt Type Register .....	6-23
6.3.5.5	FDC DMA Channel Register .....	6-23
6.3.5.6	FDC Special Configuration Register – 1 .....	6-24
6.3.5.7	FDC Special Configuration Register - 2 .....	6-24
6.3.6	IT8761E Mouse PnP Registers (LDN=04h) .....	6-25
6.3.6.1	Mouse Function Enable Control Register .....	6-25
6.3.6.2	Mouse Interrupt Control Register .....	6-25
6.3.6.3	Mouse Interrupt Type Register .....	6-26
6.3.6.4	Mouse Special Configuration Register .....	6-26
6.4	GPIO Functional Registers Description .....	6-27
<b>7.</b>	<b>Characteristics .....</b>	<b>7-1</b>
7.1	DC Electrical Characteristics .....	7-1
7.2	AC Characteristics .....	7-3
7.3	Waveform .....	7-4
<b>8.</b>	<b>Package Information .....</b>	<b>8-1</b>
<b>9.</b>	<b>Ordering Information .....</b>	<b>9-1</b>

## FIGURES

Figure 2-1.	IC Block Diagram .....	2-1
Figure 3-1.	IT8761E Pin Diagram (Top View) .....	3-1
Figure 5-1.	LPC Interface .....	5-2
Figure 5-2.	Logic Diagrams of GPIO1X and GPIO2X .....	5-3
Figure 6-1.	ISA PnP Register Map .....	6-1
Figure 6-2.	IT8761E PnP Entry/Exit Sequence .....	6-5

## TABLES

Table 4-1. LPC Bus Interface Signals .....	4-1
Table 4-2. KBC/Misc. Interface Signals.....	4-1
Table 4-3. GPIO/Mouse/FDC Interface Signals.....	4-2
Table 4-4. UART Interface Signals and Chip Test Control.....	4-4
Table 4-5. Power Signals.....	4-4
Table 4-6. IT8761E Pins Listed in Numeric Order .....	4-5
Table 5-5-1. Reset Strapping Options .....	5-1
Table 5-2. IT8761E Chip Test Mode .....	5-4
Table 5-3. XOR Chain Order.....	5-5
Table 6-1. IT8761E PnP Register Map.....	6-2
Table 7-1. Recommended Operating Conditions.....	7-1
Table 7-2. General DC Characteristics.....	7-1
Table 7-3. DC Electrical Characteristics for 5V Interface ( $T_{OPT}=0^{\circ}C\sim70^{\circ}C$ , $VCC=4.75V\sim5.25V$ ).....	7-2
Table 7-4. DC Electrical Characteristics for 3.3V Interface ( $T_{OPT}=0^{\circ}C\sim70^{\circ}C$ , $V33=3.0V\sim3.6V$ ).....	7-2
Table 7-5. AC Characteristics ( $VCC=5.0V\pm5\%$ , $V33=3.3V\pm5\%$ , $T_a=0^{\circ}C\sim70^{\circ}C$ , $C_L=87pF$ ) unit: ns .....	7-3

## 1. Features

### ■ Low Pin Count Interface

- Comply with Intel LPC Interface Specification Rev.1.0 (Sept. 29, 1997)
- Supports SERIRQ Protocol

### ■ Register sets compatible with “Plug and Play ISA Specification Rev. 1.0a”

### ■ UART

- Supports one 16C550 compatible serial port
- Maximum data rate up to 1.5 Mbps

### ■ Keyboard/Mouse Controller

- Fully 8042 compatible
- 2KB of custom ROM & 256-byte data RAM
- Supports PS/2 Keyboard and PS/2 Mouse
- Supports Keyboard GateA20 and Keyboard Reset

### ■ 16 General Purpose Input / Output Pins

- Can be individually enabled or disabled via software configuration registers
- Can be individually set as input or output via software configuration registers

- Supports four programmable De-bouncing inputs and two Blinking outputs

### ■ Floppy Disk Controller

- Supports one 360K/ 720K/ 1.2M/ 1.4M/ 2.88M floppy disk drive
- Enhanced digital data separator
- 3-Mode drive supported
- Supports software write protection
- FDC signals multiplexed with GPIO pins

### ■ Design For Testability

- Provides tri-state mode for all pins
- Supports XOR tree test mode

### ■ 33 MHz LPC Clock Input

### ■ 48 MHz System Clock Input

### ■ +3.3V (LPC) & +5V (Core) Power Supplies

### ■ Package: 48-pin LQFP

## 2. General Description

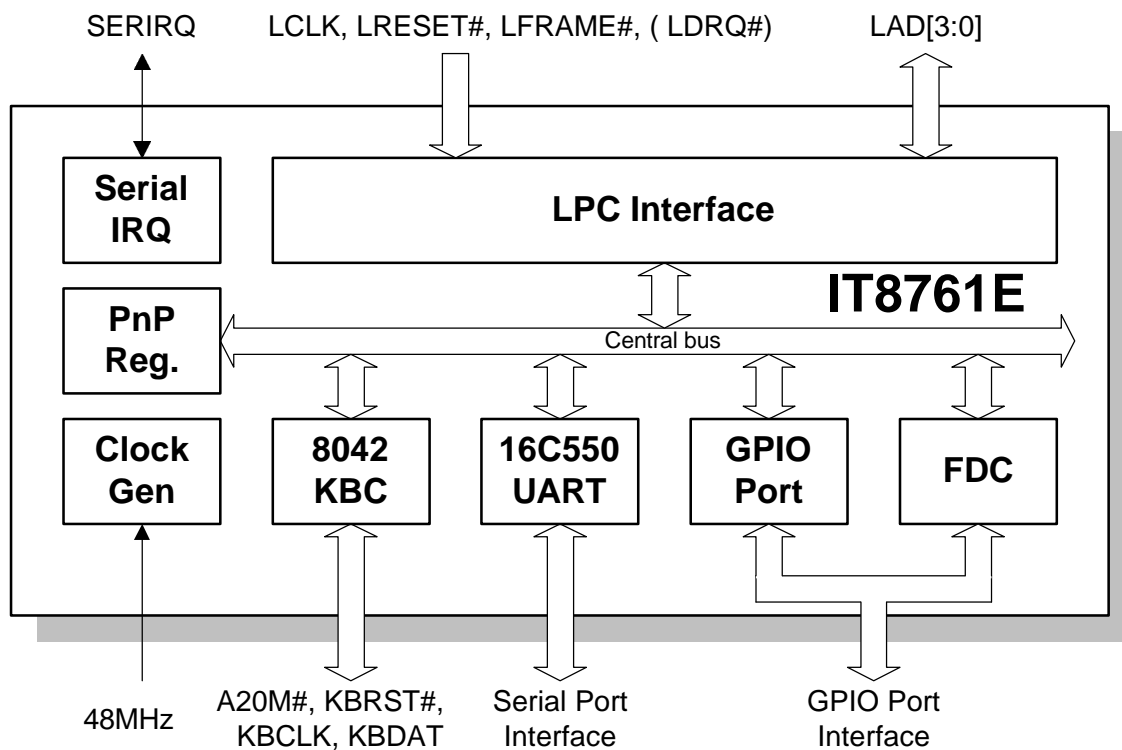
The IT8761E is a LPC Interface based Super I/O with concise legacy support for Flex ATX platform design to reduce the cost of unnecessary legacy burden. The LPC interface complies with Intel “LPC Interface Specification Rev. 1.0 (Sept. 29, 1997)”.

The IT8761E consists of one 8042 Keyboard / Mouse Controller, one 16C550 UART, one 16-pin GPIO port and one Floppy Disk Controller (Signals multiplexed with GPIO pins) logical devices. The IT8761E complies with the “Microsoft® PC98 & PC99 System Design Guide” requirements. The device requires 33MHz LPC clock and 48 MHz system clock inputs. IT8761E operates at +5V for Super I/O core & +3.3V for LPC Interface power supplies.

The IT8761E has built-in tri-state & XOR tree test modes to increase board level testability.

These five logical devices can be individually enabled or disabled via software configuration registers. The IT8761E utilizes power-saving circuitry to reduce power consumption. Once a logical device is disabled, its inputs are gated inhibited, outputs are tri-state, and the input clock is disabled.

The IT8761E is available in 48-pin LQFP package.



**Figure 2-1. IC Block Diagram**



### 3. Pin Configuration

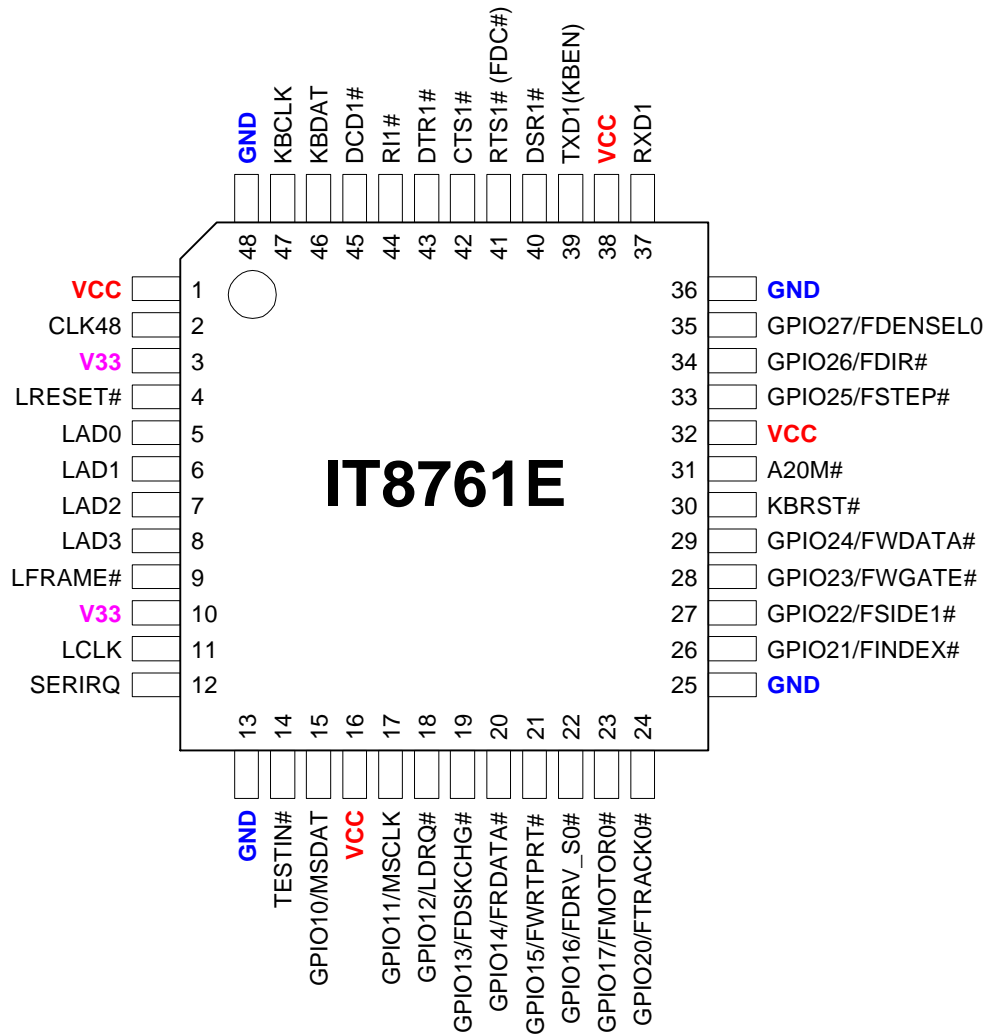


Figure 3-1. IT8761E Pin Diagram (Top View)

#### 4. Pin Description

**Table 4-1. LPC Bus Interface Signals**

Pin #	Symbol	I/O	Description	Level
4	<b>LRESET#</b>	I	<b>LPC RESET #.</b>	3.3V
12	<b>SERIRQ</b>	I/O, 5mA	<b>SERIAL IRQ.</b>	3.3V
11	<b>LCLK</b>	I	<b>LPC Clock.</b> 33 MHz PCI clock input.	3.3V
9	<b>LFRAME#</b>	I	<b>LPC Frame #.</b> This signal indicates the start of the LPC cycle.	3.3V
[8:5]	<b>LAD[3:0]</b>	I/O, 5mA	<b>LPC Address/Data 3 - 0.</b> 4-bit LPC address/bi-directional data lines. LPCAD0 is the [7:0] and LPCAD3 is the [11:8].	3.3V
18	<b>GPIO12 / LDRQ#</b>	I/O, P/U 50K, 5mA	<b>General Purpose Input / Output 12 or LDRQ#.</b> The GPIO12 will be the default function at input mode for GPIO I/F. It will also be the LPC bus DMA Request message for FDC I/F. During the reset, all the GPIO1X pins will be tri-state.	3.3V

**Table 4-2. KBC/Misc. Interface Signals**

Pin #	Symbol	I/O	Description	Level
30	<b>KBRST#</b>	O, P/U 50K, 8mA	<b>Keyboard Reset #.</b>	5V
31	<b>A20M#</b>	O, P/U 50K, 8mA	<b>Address 20 Mask #.</b>	5V
47,46	<b>KBCLK, KBDAT</b>	I/OD, P/U 50K, 16mA	<b>Keyboard Clock and Data Signals.</b> These pins are <i>Keyboard Clock and Data signals</i> , and are also used to select the IT8761E testing mode. They should be No Connected if the keyboard is not in use (do not tie to VCC or GND) for normal operation in system application.	5V
2	<b>CLK48</b>	I	<b>48 MHz Clock Input.</b>	5V
14	<b>TESTIN#</b>	I, P/U 50K	<b>IC-Test-Select #.</b> This pin is used to select the IT8761E operational mode: normal mode or testing mode. It should be No Connected or tied to VCC for normal operation in system application.	5V

**Table 4-3. GPIO/Mouse/FDC Interface Signals**

Pin #	Symbol	I/O	Description	Level
15	<b>GPIO10 / MSDAT</b>	I/O, P/U 50K, 16mA	<b>General Purpose Input / Output 10 / Mouse DATA.</b> The GPIO10 will be defaulted at input mode. This pin is MUX-ed with MSDAT. During the reset, all the GPIO1X pins will be TRI-STATE.	5V
17	<b>GPIO11 / MSCLK</b>	I/O, P/U 50K, 16mA	<b>General Purpose Input / Output 11 / Mouse CLK.</b> The GPIO11 will be defaulted at input mode. This pin is MUX-ed with MSCLK. During the reset, all the GPIO1X pins will be TRI-STATE.	5V
19	<b>GPIO13 / FDSKCHG#</b>	I/O, P/U 50K, 8mA	<b>General Purpose Input / Output 13 / FDSKCHG#.</b> The GPIO13 will be defaulted at input mode for GPIO I/F. It is MUX-ed with the Floppy Disk Change status input for FDC I/F. During the reset, all the GPIO1X pins will be TRI-STATE.	5V
20	<b>GPIO14 / FRDATA#</b>	I/O, P/U 50K, 8mA	<b>General Purpose Input / Output 14 / FRDATA#.</b> The GPIO14 will be defaulted output high for GPIO I/F. It is MUX-ed with the Floppy Disk Read Data input for FDC I/F. During the reset, all the GPIO1X pins will be TRI-STATE.	5V
21	<b>GPIO15 / FWRTPR#</b>	I/O, P/U 50K, 8mA	<b>General Purpose Input / Output 15 / FWRTPR#.</b> The GPIO15 will be defaulted output high for GPIO I/F. It is MUX-ed with the Floppy Disk Write protect status input for FDC I/F. During the reset, all the GPIO1X pins will be TRI-STATE.	5V
22	<b>GPIO16 / FDRV_S0#</b>	I/O, P/U 50K, 24mA	<b>General Purpose Input / Output 16 / FDRV_S0#.</b> The GPIO16 will be defaulted output high for GPIO I/F. It is MUX-ed with the Floppy Drive Select (Enable) output for FDC I/F. During the reset, all the GPIO1X pins will be TRI-STATE.	5V
23	<b>GPIO17 / FMOTOR0#</b>	I/O, P/U 50K, 24mA	<b>General Purpose Input / Output 17 / FMOTOR0#.</b> The GPIO17 will be defaulted output high for GPIO I/F. It is MUX-ed with the Floppy Drive Motor Enable output for FDC I/F. During the reset, all the GPIO1X pins will be TRI-STATE.	5V

Pin #	Symbol	I/O	Description	Level
24	<b>GPIO20 / FTRACK0#</b>	I/O, P/U 50K, 8mA	<b>General Purpose Input / Output 20 / FTRACK0#.</b> The GPIO20 will be defaulted output low for GPIO I/F. It is MUX-ed with the FDD Track 0 input for FDC I/F. During the reset, all the GPIO2X pins will be TRI-STATE.	5V
26	<b>GPIO21 / FINDEX#</b>	I/O, P/U 50K, 8mA	<b>General Purpose Input / Output 21 / FINDEX#.</b> The GPIO21 will be defaulted output low for GPIO I/F. It is MUX-ed with the FDD Track beginning indicator status for FDC I/F. During the reset, all the GPIO2X pins will be TRI-STATE.	5V
27	<b>GPIO22 / FSIDE1#</b>	I/O, P/U 50K, 24mA	<b>General Purpose Input / Output 22 / FSIDE1#.</b> The GPIO22 will be defaulted output low for GPIO I/F. It is MUX-ed with the FDD Head Select output (Side1) for FDC I/F. During the reset, all the GPIO2X pins will be TRI-STATE.	5V
28	<b>GPIO23 / FWGATE#</b>	I/O, P/U 50K, 24mA	<b>General Purpose Input / Output 23 / FWGATE#.</b> The GPIO23 will be defaulted output low for GPIO I/F. It is MUX-ed with the FDD Write Gate Enable output for FDC I/F. During the reset, all the GPIO2X pins will be TRI-STATE.	5V
29	<b>GPIO24 / FWDATA#</b>	I/O, P/U 50K, 24mA	<b>General Purpose Input / Output 24 / FWDATA#.</b> The GPIO24 will be defaulted output low for GPIO I/F. It is MUX-ed with the FDD Write Serial Data output for FDC I/F. During the reset, all the GPIO2X pins will be TRI-STATE.	5V
33	<b>GPIO25 / FSTEP#</b>	I/O, P/U 50K, 24mA	<b>General Purpose Input / Output 25 / FSTEP#.</b> The GPIO25 will be defaulted output low for GPIO I/F. It is MUX-ed with the FDD Step Pulse output for FDC I/F. During the reset, all the GPIO2X pins will be TRI-STATE.	5V
34	<b>GPIO26 / FDIR#</b>	I/O, P/U 50K, 24mA	<b>General Purpose Input / Output 26 / FDIR#.</b> The GPIO26 will be defaulted output low for GPIO I/F. It is MUX-ed with the FDD Head Step Direction output for FDC I/F (0 for Step-In; 1 for Step-Out in SEEK operation). During the reset, all the GPIO2X pins will be TRI-STATE.	5V
35	<b>GPIO27 / FDENSEL0</b>	I/O, P/U 50K, 24mA	<b>General Purpose Input / Output 27 / FDENSEL0.</b> The GPIO27 will be defaulted output low for GPIO I/F. It is MUX-ed with the FDD Density Select output for FDC I/F (0 for 250K / 300Kbps; 1 for 500K / 1Mbps). During the reset, all the GPIO2X pins will be TRI-STATE.	5V

**Table 4-4. UART Interface Signals and Chip Test Control**

Pin #	Symbol	I/O	Description	Level
37	RXD1	I, P/U 50K	<b>Serial Data In 1.</b> This input receives serial data from the communications link.	5V
39	TXD1 (KBEN)	I/O, P/U 50K, 8mA	<b>Serial Data Out 1.</b> This output sends serial data to the communications link. This signal is set to a marking state (logic 1) after a Master Reset operation.  <i>* During RESET, this pin is input for KBEN Reset-strapping option.</i>	5V
40	DSR1#	I, P/U 50K	<b>Data Set Ready 1 #.</b> When low, indicates that the MODEM or data set is ready to establish a communications link. The DSR1# signal is a MODEM status input whose condition can be tested by reading the MSR register.	5V
41	RTS1# (FDC#)	O, P/U 50K, 8mA	<b>Request to Send 1 #.</b> When low, this output indicates to the MODEM or data set that the device is ready to send data. RTS1# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, RTS1# is set to its inactive state.  <i>* During RESET, this pin is input for FDC interface (if P/D) or GPIO interface (if P/U) Reset-strapping option.</i>	5V
42	CTS1#	I, P/U 50K	<b>Clear to Send 1 #.</b> When low, indicates that the MODEM or data set is ready to accept data. The CTS1# signal is a MODEM status input whose condition can be tested by reading the MSR register.	5V
43	DTR1#	O, P/U 50K, 8mA	<b>Data Terminal Ready 1 #.</b> DTR1# is used to indicate to the MODEM or data set that the device is ready to exchange data. DTR1# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, DTR is set to its inactive state.	5V
44	RI1#	I, P/U 50K	<b>Ring Indicator 1 #.</b> When the signal is low, it indicates that a telephone ring signal has been received by the MODEM. The RI1# signal is a MODEM status input whose condition can be tested by reading the MSR register.	5V
45	DCD1#	I, P/U 50K	<b>Data Carrier Detect 1 #.</b> When the signal is low, it indicates that the MODEM or data set has detected a carrier. The DCD1# signal is a MODEM status input whose condition can be tested by reading the MSR register.	5V

**Table 4-5. Power Signals**

Pin #	Symbol	I/O	Description	Level
1, 16, 32, 38	VCC	PWR	<b>5V Power Pins.</b>	5V
3, 10	V33	PWR	<b>3.3V Power Pins.</b>	3.3V
13, 25, 36, 48	GND	PWR	<b>Ground Pins.</b>	0 V

**Table 4-6. IT8761E Pins Listed in Numeric Order**

Pin	Symbol
1	VCC
2	CLK48
3	V33
4	LRESET#
5	LAD0
6	LAD1
7	LAD2
8	LAD3
9	LFRAME#
10	V33
11	LCLK
12	SERIRQ

Pin	Symbol
13	GND
14	TESTIN#
15	GPIO10/MSDAT
16	VCC
17	GPIO11/MSCLK
18	GPIO12/LDRQ#
19	GPIO13/FDSKCHG#
20	GPIO14/FRDATA#
21	GPIO15/FWRTPT#
22	GPIO16/FDRV_S0#
23	GPIO17/FMOTOR0#
24	GPIO20/FTRACK0#

Pin	Symbol
25	GND
26	GPIO21/FINDEX#
27	GPIO22/FSIDE1#
28	GPIO23/FWGATE#
29	GPIO24/FWDATA#
30	KBRST#
31	A20M#
32	VCC
33	GPIO25/FSTEP#
34	GPIO26/FDIR#
35	GPIO27/FDENSEL0
36	GND

Pin	Symbol
37	RXD1
38	VCC
39	TXD1 (KBEN)
40	DSR1#
41	RTS1# (FDC#)
42	CTS1#
43	DTR1#
44	RI1#
45	DCD1#
46	KBDAT
47	KBCLK
48	GND

## 5. Functional Description

### 5.1 Reset Strapping Options

The IT8761E operation mode is latched when the LRESET# (pin #4) is de-asserted.

**Table 5-1. Reset Strapping Options**

Pin No.	Symbol	Value	Description
39	<b>TXD1</b> (KBEN: for KBC Enabling)	1	Keyboard Controller is enabled after Reset. (Default) The TXD1 signal has an internal 50K Ohm pull-up resistor.
		0	Keyboard Controller is disabled after Reset. The recommended pull-down resistor value is 1K Ohm to 5K Ohm
41	<b>RTS1#</b> (FDC#: for GPIO/FDC MUX Select)	1	GPIO function selected. (Default) The RTS1# has an internal 50K Ohm pull-up resistor.
		0	FDC function selected. The recommended pull-down resistor value is 1K Ohm to 5K Ohm.

### 5.2 LPC Interface

#### 5.2.1 Overview

Instead of supporting the traditional ISA Bus, the IT8761E complies with the Intel LPC interface. The LPC interface provides much less pin counts, but more efficient transaction timings. For detailed LPC protocol, please refer to the Intel "Low Pin Count (LPC) Interface Specification, Revision 1.0, September 29,1997".

#### 5.2.2 LPC Transactions

The LPC interface of the IT8761E supports LPC Host I/O read/write transactions for the Super I/O module.

For LPC Host I/O read or write transactions, the Super I/O module uses a positive decode. The LPC interface depends on the decoding result to respond to the current transaction by sending out SYNC values on LAD[3:0] signals or leave LAD[3:0] to tri-state.

### 5.2.3 LPC I/F Block Diagram

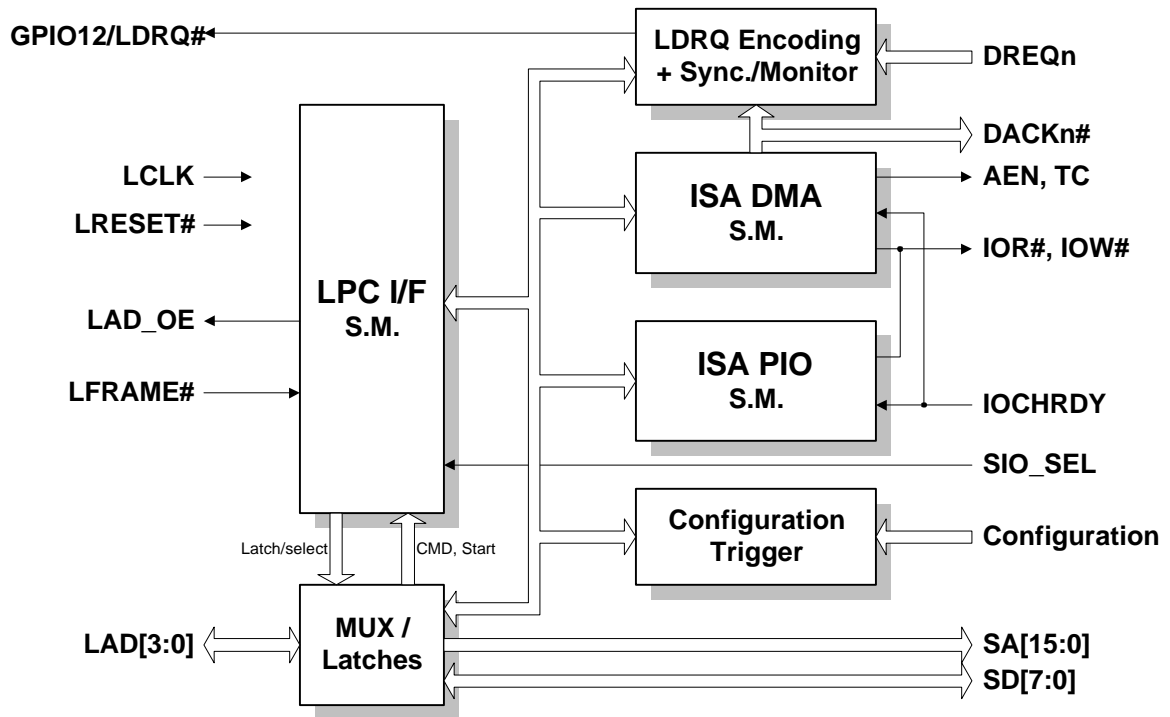
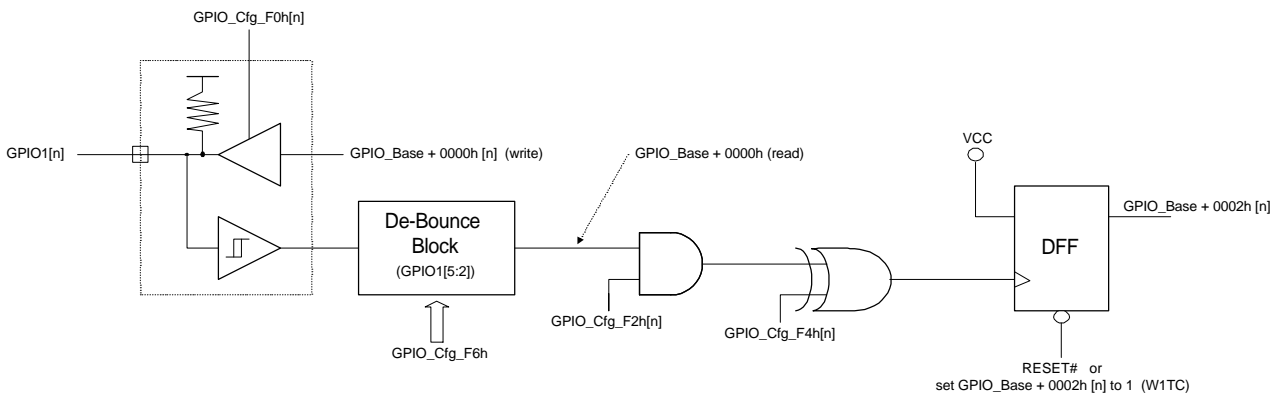


Figure 5-1. LPC Interface

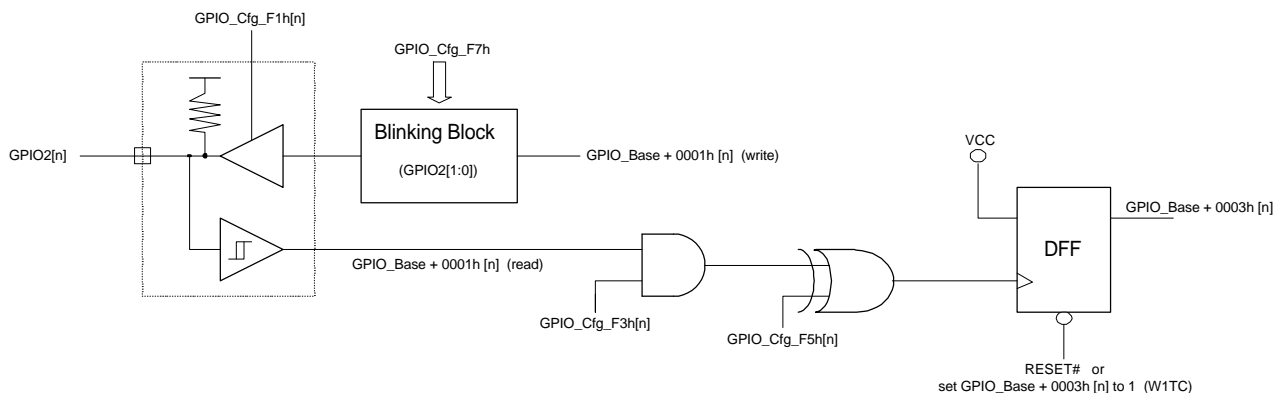


### 5.3 GPIO

Illustrated below are the equivalent logic diagrams of GPIO1[7:0] and GPIO2[7:0] controls. Four independent De-Bounce options of GPIO1[5:2] inputs are provided for system makers to implement Push Button or Switch inputs. Two Blinking options of GPIO2[1:0] outputs are also made available for system makers to implement LED blinking for system operation mode indications.



**GPIO1X Logics**



**GPIO2X Logics**

**Figure 5-2. Logic Diagrams of GPIO1X and GPIO2X**

## 5.4 Testability

The IT8761E builds some test modes for the purpose of chip testing, not for system testing.

**Table 5-2. IT8761E Chip Test Mode**

Operation Mode	TESTIN#	KBDAT	KBCLK	Description
XOR-Chain Mode	0	1	0	Test connection of the IT8761E on board, IC $V_{IH}/V_{IL}$ .
Chip Tri-State Mode	0	1	1	Test connection of other chips on board.
KBC Test Mode	0	0	0	For Chip on ATE testing.
Normal Operation	0	0	1	Reserved
Normal Operation	1	X	X	

### Tri-State Test:

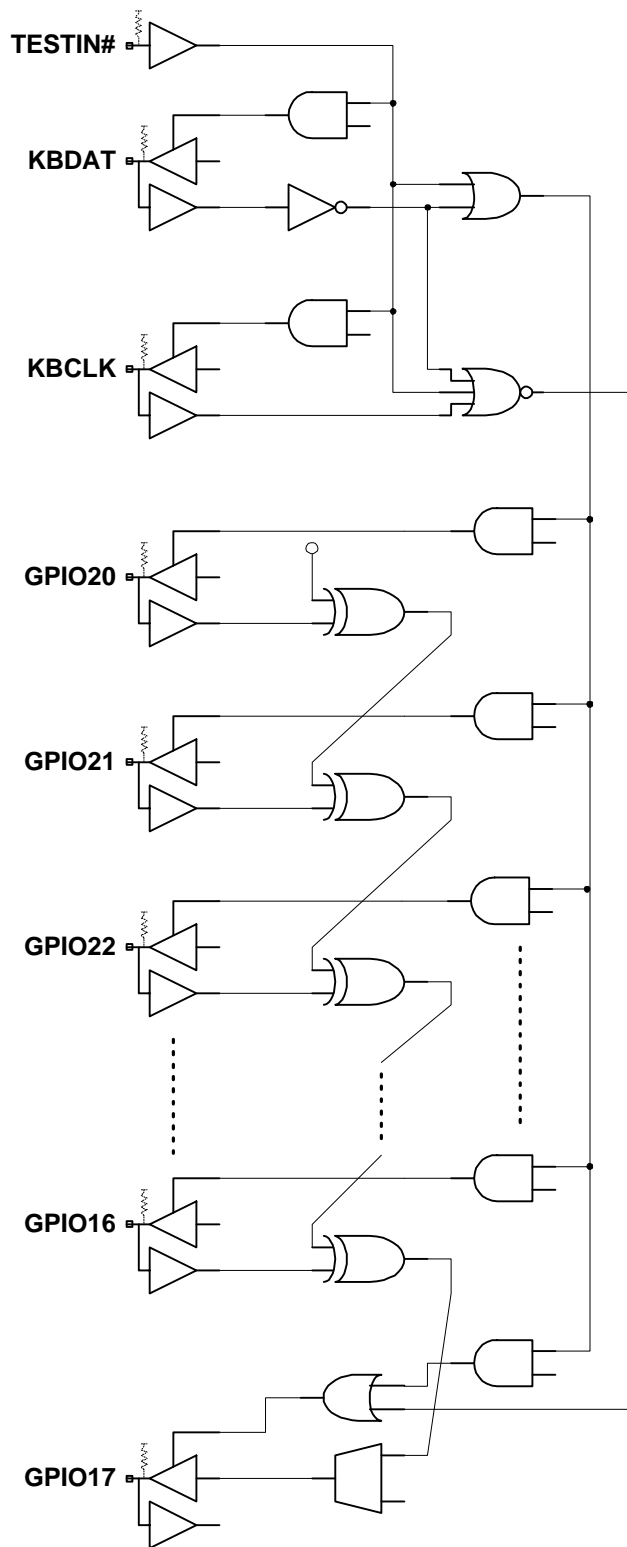
This test mode tri-states all outputs and bi-directional buffers, including the XOR chain output: GPIO17.

### XOR Chain Test:

This test mode tri-states all outputs and bi-directional buffers, except the GPIO17. The outputs (not including GPIO17) are configured as inputs in the XOR chain. The first input of the XOR chain is GPIO20. The XOR chain is routed counter-clockwise around the chip (e.g., GPIO20, GPIO21, GPIO22,...). GPIO17 is the XOR chain output. TESTIN#, KBDAT, KBCLK, and GPIO17 pins are not included in the XOR chain. This testing can be used to verify the chip package connectivity and  $V_{IH}/V_{IL}$  DC characteristics.

**Table 5-3. XOR Chain Order**

Pin #	Signal Name	Note	Pin #	Signal Name	Note
1	VCC		25	GND	
2	CLK48	XOR Chain – 19 <sup>th</sup>	26	GPIO21/FINDEX#	XOR Chain – 2 <sup>nd</sup>
3	V33		27	GPIO22/FSIDE1#	XOR Chain – 3 <sup>rd</sup>
4	LRESET#	XOR Chain – 20 <sup>th</sup>	28	GPIO23/FWGATE#	XOR Chain – 4 <sup>th</sup>
5	LAD0	XOR Chain – 21 <sup>st</sup>	29	GPIO24/FWDATA#	XOR Chain – 5 <sup>th</sup>
6	LAD1	XOR Chain – 22 <sup>nd</sup>	30	KBRST#	XOR Chain – 6 <sup>th</sup>
7	LAD2	XOR Chain – 23 <sup>rd</sup>	31	A20M#	XOR Chain – 7 <sup>th</sup>
8	LAD3	XOR Chain – 24 <sup>th</sup>	32	VCC	
9	LFRAME#	XOR Chain – 25 <sup>th</sup>	33	GPIO25/FSTEP#	XOR Chain – 8 <sup>th</sup>
10	V33		34	GPIO26/FDIR#	XOR Chain – 9 <sup>th</sup>
11	LCLK	XOR Chain – 26 <sup>th</sup>	35	GPIO27/FDENSEL0	XOR Chain – 10 <sup>th</sup>
12	SERIRQ	XOR Chain – 27 <sup>th</sup>	36	GND	
13	GND		37	RXD1	XOR Chain – 11 <sup>th</sup>
14	TESTIN#	Set to 0 for test mode	38	VCC	
15	GPIO10/MSDAT	XOR Chain – 28 <sup>th</sup>	39	TXD1 (KBEN)	XOR Chain – 12 <sup>th</sup>
16	VCC		40	DSR1#	XOR Chain – 13 <sup>th</sup>
17	GPIO11/MSCLK	XOR Chain – 29 <sup>th</sup>	41	RTS1# (FDC#)	XOR Chain – 14 <sup>th</sup>
18	GPIO12/LDRQ#	XOR Chain – 30 <sup>th</sup>	42	CTS1#	XOR Chain – 15 <sup>th</sup>
19	GPIO13/FDSKCHG#	XOR Chain – 31 <sup>st</sup>	43	DTR1#	XOR Chain – 16 <sup>th</sup>
20	GPIO14/FRDATA#	XOR Chain – 32 <sup>nd</sup>	44	RI1#	XOR Chain – 17 <sup>th</sup>
21	GPIO15/FWRTPT#	XOR Chain – 33 <sup>rd</sup>	45	DCD1#	XOR Chain – 18 <sup>th</sup>
22	GPIO16/FDRV_S0#	XOR Chain – 34 <sup>th</sup>	46	KBDAT	Set to 1 for XOR Chain Test Mode
23	GPIO17/FMOTOR0#	XOR Chain Output	47	KBCLK	Set to 0 for XOR Chain Test Mode
24	GPIO20/FTRACK0#	Chain Start Point – 1 <sup>st</sup>	48	GND	



**Figure 5-3. XOR Chain**

## 6. Register Description

### 6.1 Standard ISA Plug-and-Play (PnP) High Level Register Map

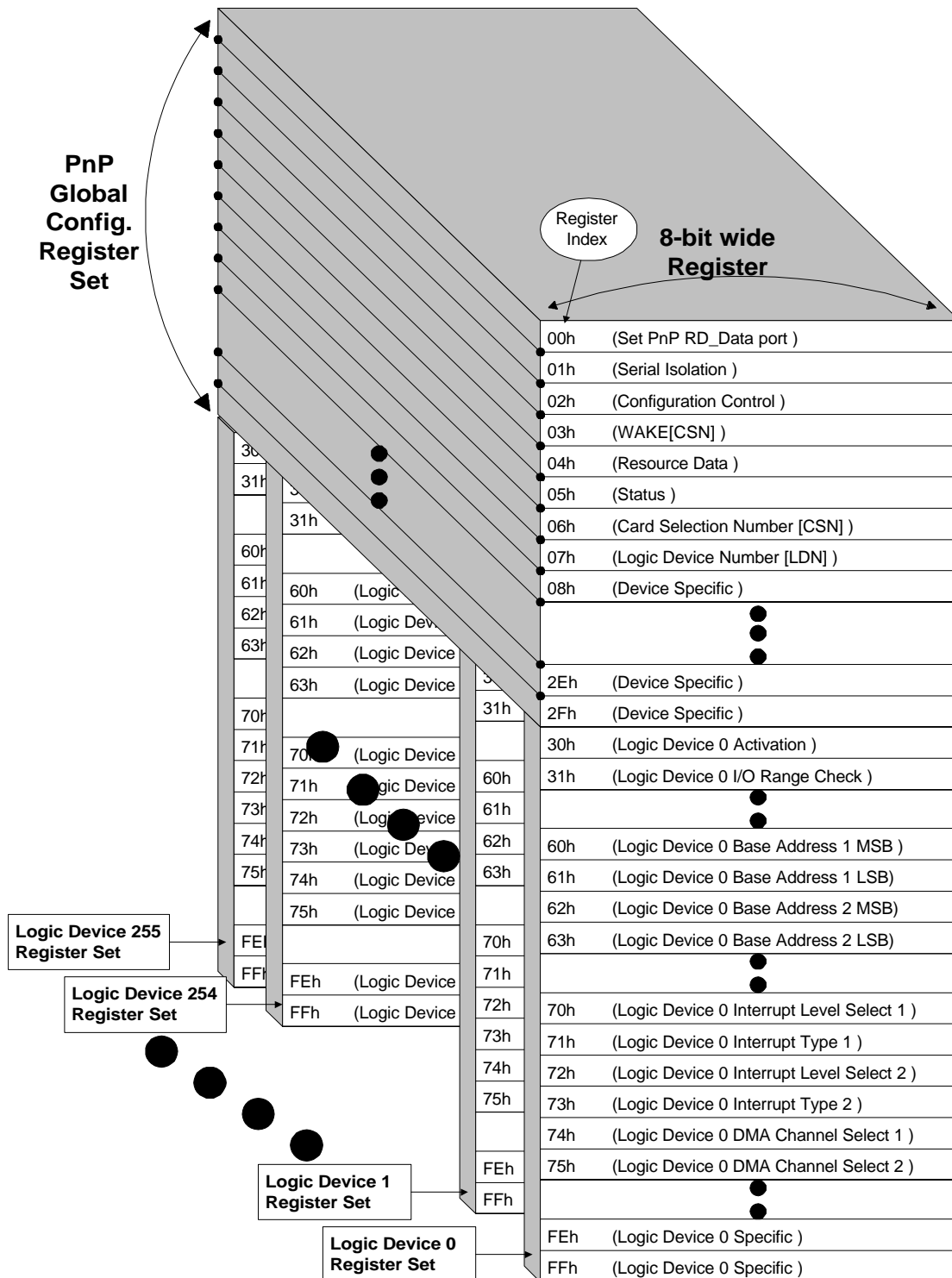


Figure 6-1. ISA PnP Register Map

**Table 6-1. IT8761E PnP Register Map**

LDN	Index	R/W	Default(Hex)	Register Descriptions
<b>Global (LDN=XXh)</b>	02	W	NA	Configure Control
	07	R/W	NA	Logical Device Number(LDN)
	20	R	87	Chip ID Byte 1
	21	R	61	Chip ID Byte 2
	22	R	00	Chip Version
	23	R/W	44	LPC to X-bus PIO Timing Register
	24	R/W	F0	LPC to X-bus DMA Timing Register - 1
	25	R/W	FC	LPC to X-bus DMA Timing Register – 2
	2E	R/W	00	Chip Test Mode Enable Register
	others	RO	00	Reserved
<b>KBC (LDN=00h)</b>	30	R/W	00 / 01	KBC Function Enable Control Register 00h: Disabled after reset strapping pin TXD1 (P/D) 01h: Enabled after reset strapping pin TXD1 (no Pull)
	60	R/W	00	KBC Module Data Port Base Address [15:8] Register
	61	R/W	60	KBC Module Data Port Base Address [7:0] Register
	62	R/W	00	KBC Module Command Port Base Address [15:8] Register
	63	R/W	64	KBC Module Command Port Base Address [7:0] Register
	70	R/W	01	KBC Interrupt Control Register
	71	R/W	02	KBC Interrupt Type Register
	F0	R/W	00	KBC Special Configuration Register
	F1	R/W	7F	Reserved (Emulated KBC Host Interface Control Register)
<b>UART (LDN=01h)</b>	30	R/W	00	UART Function Enable Control Register
	60	R/W	03	UART Module Base Address [15:8] Register
	61	R/W	F8	UART Module Base Address [7:0] Register
	70	R/W	04	UART Interrupt Control Register
	71	R/W	02	UART Interrupt Type Register
	F0	R/W	00	UART Special Configuration Register

LDN	Index	R/W	Default(Hex)	Register Descriptions
<b>GPIO (LDN=02h)</b>	60	R/W	02	GPIO Base Address [15:8] Register
	61	R/W	90	GPIO Base Address [7:0] Register
	70	R/W	00	GPIO Interrupt Control Register
	71	R/W	02	GPIO Interrupt Type Register
	F0	R/W	F0	GPIO1X Input / Output Selection Register
	F1	R/W	FF	GPIO2X Input / Output Selection Register
	F2	R/W	00	GPIO1X Input Interrupt Mask Register
	F3	R/W	00	GPIO2X Input Interrupt Mask Register
	F4	R/W	00	GPIO1X Interrupt Trigger Edge Register
	F5	R/W	00	GPIO2X Interrupt Trigger Edge Register
	F6	R/W	00	GPIO De-bounce Register
	F7	R/W	00	GPIO Blinking Register
	F8	R/W	00	Software Interrupt Trigger Enable Register - 1
	F9	R/W	00	Software Interrupt Trigger Enable Register - 2
	FA	R/W	00	Software Interrupt Trigger Register - 1
	FB	R/W	00	Software Interrupt Trigger Register - 2
	FE	R/W	00	GPIO Special Configuration Register
<b>FDC (LDN=03h)</b>	30	R/W	00	FDC Function Enable Control Register
	60	R/W	03	FDC Module Base Address [15:8] Register
	61	R/W	F0	FDC Module Base Address [7:0] Register
	70	R/W	06	FDC Interrupt Control Register
	71	R/W	02	FDC Interrupt Type Register
	74	R/W	02	FDC DMA Channel Register
	F0	R/W	0C	FDC Special Configuration Register - 1
	FE	R/W	00	FDC Special Configuration Register - 2
<b>Mouse (LDN=04h)</b>	30	R/W	00	Mouse Function Enable Control Register
	70	R/W	0C	Mouse Interrupt Control Register
	71	R/W	02	Mouse Interrupt Type Register
	F0	R/W	00	Mouse Special Configuration Register

## 6.2 Global Configuration Register Set Description

The Global Configuration Register Set contains the registers from the index 00h to 2Fh in the ISA Plug-and-Play register map. Some specific functional control registers are defined by the ISA Plug-and-Play Specification, Rev. 1.0. These registers are accessed through the index-data scheme described in the ISA Plug-and-Play Specification v1.0. This LPC Super I/O implements the majority of the registers required by the Motherboard Plug-and-Play.

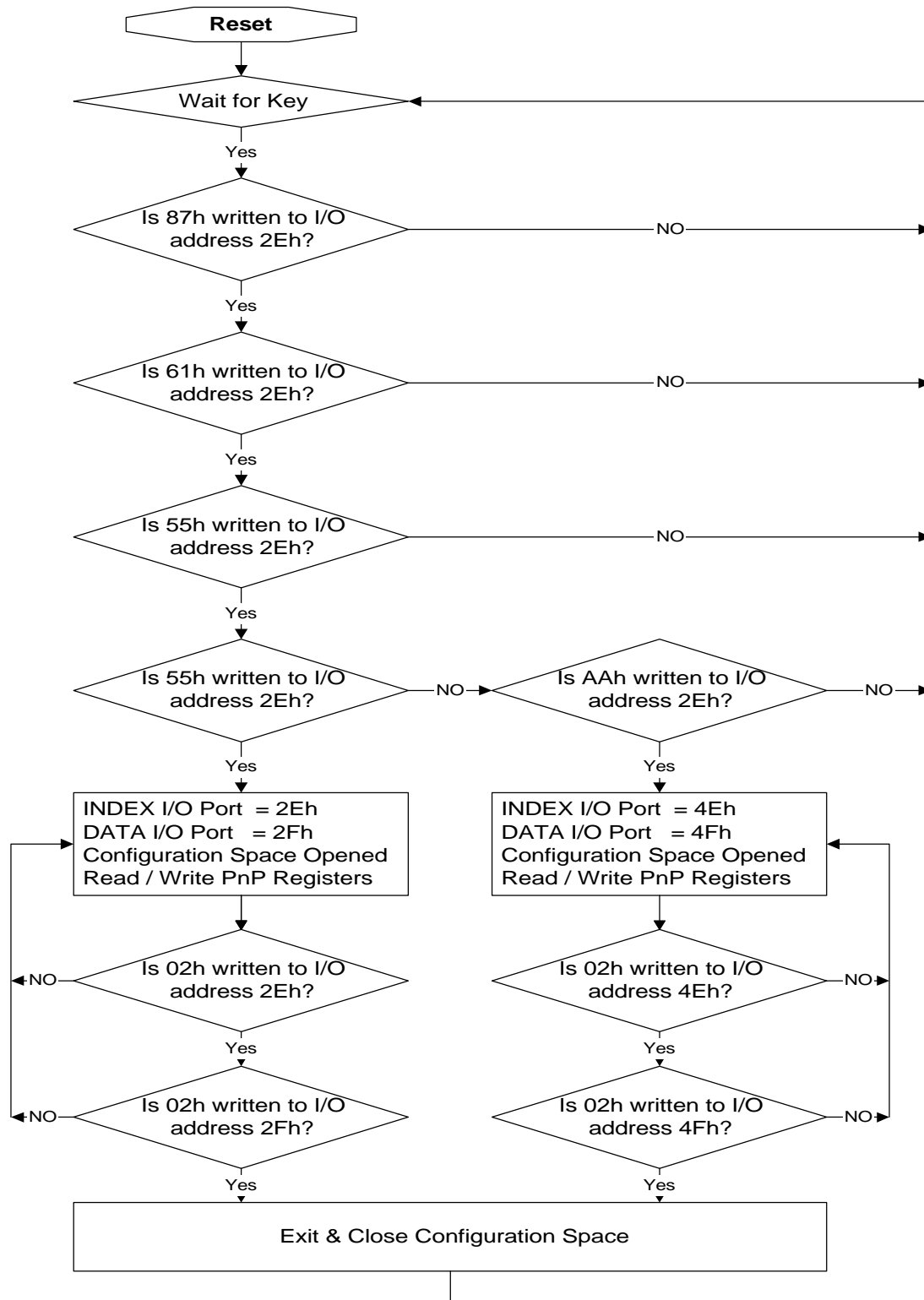
All the registers will be reset to the default values when the hardware reset signal is activated or the software reset command is issued. The software reset command is issued to the bit 0 of the Configure Control register (PnP Index = 02h).

The LPC Super I/O configuration registers can be accessed through an index-data I/O pair that only requires two I/O addresses. There are two possible index-data I/O pair locations for this chip: 2Eh/2Fh or 4Eh/4Fh.

The index-data I/O pair selection can be decided through a 4 sequentially I/O writes (does not have to be a continuous I/O write) to the targeted Index I/O address. In order to enter the LPC Super I/O configuration mode, the software needs to write 4 designed bytes (87h, 61h, 55h, 55h to I/O address 2Eh or 87h, 61h, 55h, AAh to I/O address 4Eh) to select the index-data pair and open the configuration space. In order to prevent any mis-writes to the PnP registers, the configuration space can be closed by writing 02h to the Index I/O port followed by another 02h write to the data I/O port.

The flow chart on the next page illustrates the software configuration sequence:





**Figure 6-2. IT8761E PnP Entry/Exit Sequence**

### 6.3 PnP Configuration Registers Description

Below is the register description format:

Index Value		Register Function	
register bits	R/W attribute	Register bits description.	Default value

#### 6.3.1 IT8761E Global PnP Registers

##### 6.3.1.1 Configure Control Register

This is a **write only** register used to exit PnP Configure Sequence. Following the entry of the IT8761E Configuration Sequence, the BIOS/driver should set this Global\_Cfg\_02h<1> to 1 as it processes some PnP register settings. By doing so, the BIOS/driver can exit PnP Configuration Sequence safely, and avoids future PnP programming of other chips that might result in some undesirable effects on the IT8761E register settings.

Global_Cfg_02h		Configure Control Register	
<7:2>	WO	Reserved	-
<1>	WO	<b>Exit Configure Sequence:</b> 0: No Operation.      1: Exit.	-
<0>	WO	Reserved	-

##### 6.3.1.2 Logical Device Number Register

This register should be programmed with a proper Logical Device number before the future configuration on the dedicated Logical Device in the IT8761E.

Global_Cfg_07h		Logical Device Number Register	
<7:0>	R/W	<b>Select Logical Device:</b> 00h: PS/2 KBC.      01h: UART.      02h: GPIO. 03h: FDC.      04h: PS/2 Mouse.      others: Reserved.	FFh

##### 6.3.1.3 Chip ID Number Register

The Global\_Cfg\_20h & Global\_Cfg\_21h are used to identify the Chip ID is "8761."

Global_Cfg_20h		Chip ID Number Register Byte 1	
<7:0>	RO	IT8761E Chip ID Number: Byte 1.	87h

Global_Cfg_21h		Chip ID Number Register Byte 2	
<7:0>	RO	IT8761E Chip ID Number: Byte 2.	61h

#### 6.3.1.4 Chip Version Number Register

This register is provided for BIOS/Driver to identify the chip version.

Global_Cfg_22h		Chip Version Number Register	
<7:0>	RO	IT8761E Chip Version Number.	00h

#### 6.3.1.5 LPC to X-bus PIO Timing Register

The Global\_Cfg\_23h is used to adjust the setup/active time of LPC PIO cycle, ensuring a better IT8761E LPC interface performance. Those setting values cover from the slowest legacy ISA timing (IEEE P996 draft) to minimum LPC latency of PIO transactions.

Global_Cfg_23h		LPC to X-bus PIO Timing Register	
<7>	R/W	PIO cycle SA to IOR# setup time. 0: Slow. 1: Fast.	0b
<6:4>	R/W	PIO cycle IOR# Active time (4*LCLKs + Value*2*LCLKs). For example: the value of 000b is 4*LCLKs, and 111b is 18*LCLKs.	100b
<3>	R/W	PIO cycle SA to IOW# setup time. 0: Slow. 1: Fast.	0b
<2:0>	R/W	PIO cycle IOW# Active time (4*LCLKs + Value*2*LCLKs). For example: the value of 000b is 4*LCLKs, and 111b is 18*LCLKs.	100b

#### 6.3.1.6 LPC to X-bus DMA Timing Register

These registers are used to adjust the setup/active time of LPC DMA cycle, ensuring a better IT8761E LPC interface performance. Those setting values cover from the slowest legacy ISA timing (IEEE P996 draft) to minimum LPC latency of DMA transactions.

- Global\_Cfg\_24h<7:6> & Global\_Cfg\_24h<5:4> are the programmable setup time of AEN/DACKn# to IOR#/IOW# for DMA devices.
- Global\_Cfg\_24h<3:0> is reserved and should leave it at 0000b.
- Global\_Cfg\_25h<7:4> & Global\_Cfg\_25h<3:0> are the programmable IOR#/IOW# active time for DMA devices.

Global_Cfg_24h		LPC to X-bus DMA Timing Register - 1	
<7:6>	R/W	DMA cycle AEN/DACKn# to IOR# setup time (1*LCLK + Value*LCLKs). For example: the value of 0b is 1*LCLKs, and 11b is 4*LCLKs.	11b
<5:4>	R/W	DMA cycle AEN/DACKn# to IOW# setup time (1*LCLK + Value*LCLKs). For example: the value of 0b is 1*LCLKs, and 11b is 4*LCLKs.	11b
<3:0>	R/W	Reserved. (For testing LPC Verify mode backward compatible to Legacy DMAC-8237 Verify Transfer operation). Software mask IOR# of DMA Verify mode. Set 1 to bits<3:0> is masking relative DMA channel [3:0].	0000b

Global_Cfg_25h		LPC to X-bus DMA Timing Register - 2	
<7:4>	R/W	DMA cycle IOR# Active time (4*LCLK + Value*LCLKs). For example: the value of 0000b is 4*LCLKs, and 1111b is 19*LCLKs.	1111b
<3:0>	R/W	DMA cycle IOR# Active time (4*LCLK + Value*LCLKs). For example: the value of 0000b is 4*LCLKs, and 1111b is 19*LCLKs.	1100b

### 6.3.1.7 Chip Test Mode Enable Register

This register is left for chip testing only, and should not be programmed by users.

Global_Cfg_2Eh		Chip Test Mode Enable Register	
<7:5>	R/W	FDC Test mode[3:1] (for chip test only).	000b
<4>	RO	Reserved	0b
<3>	R/W	Pin#_35 Function Select.      0: GPIO27.      1: BAUD rate output.	0b
<2>	R/W	Enable Chip Test Observe points (for chip test only): 0: Normal      1: Observe Outputs: Pin#_29:      GPIO24      UART_IRQ. Pin#_31:      A20M#      GPIO_IRQ. Pin#_33:      GPIO25      MOUSE_IRQ. Pin#_34:      GPIO26      KBC_IRQ.	0b
<1>	R/W	Enable Clock Dividers Testing (for chip test only): 0: Normal frequency.      1: Enable clock divider control (see bit 0).	0b
<0>	R/W	Control point in Clock Dividers (for chip test only): 0: at every 1/64 points.      1: at one flip-flop before every 1/64 points.	0b

### 6.3.1.8 Other registers not listed above with index between 00h~2Fh

Undefined registers of IT8761E Global PnP registers (Index between 00h - 2Fh) are **read only** as 00h.

Global_other		Other registers not listed above with index between 00h~2Fh	
<7:0>	RO	Reserved	00h

### 6.3.2 IT8761E KBC PnP Registers (LDN=00h)

When the Global\_Cfg\_07h is programmed as 00h in the IT8761E configuration sequence, the KBC device of the IT8761E is then selected. After the following PnP programming with index between 30h~FFh is applied to the KBC device, either the Global\_Cfg\_07h value can then be changed or the IT8761E Configuration Sequence can be exited.

#### 6.3.2.1 KBC Function Enable Control Register

The KBC\_Cfg\_30h<0> controls the enable/disable state of the IT8761E KBC function. The default KBC function enable control is set by Reset strap value (Pull/Up or Pull/Down) on TXD1 signal (pin# 39).

Since the KBC module includes an 8042 microprocessor and a boot ROM programming time (about 30μs, (microseconds) is required before the KBC can accept Self-Test command (AAh for KBC command port). During a KBC Self-Test command, some KBC operation behaviors are setup to support other KBC commands. So, BIOS/Driver should be aware of 30~50ms (milliseconds) latency.

KBC_Cfg_30h		KBC Function Enable Control Register	
<7:1>	RO	Reserved	0000000b
<0>	R/W	KBC Function Enable Control. 0: Disable.      1: Enable.	TXD1 Reset Strap value

#### 6.3.2.2 KBC Module Base Address Registers

The KBC Module contains two address ports, with each of which providing one byte space only. There is no relationship limitation between these two base address values. And these two ports are also dedicated to the Mouse device, since the PS/2 Mouse share the identical KBC Module with PS/2 Keyboard.

- KBC Data Port (default address is 0060h): KBC\_Cfg\_60h & KBC\_Cfg\_61h.
- KBC Command Port (default address is 0064h): KBC\_Cfg\_62h & KBC\_Cfg\_63h.

KBC_Cfg_60h		KBC Module Data Port Base Address Register: High Byte	
<7:0>	R/W	KBC Module Data Port Base Address: KBC_Data_BA[15:8].	00h

KBC_Cfg_61h		KBC Module Data Port Base Address Register: Low Byte	
<7:0>	R/W	KBC Module Data Port Base Address: KBC_Data_BA[7:0].	60h

KBC_Cfg_62h		KBC Module Command Port Base Address Register: High Byte	
<7:0>	R/W	KBC Module Command Port Base Address: KBC_CMD_BA[15:8].	00h

KBC_Cfg_63h		KBC Module Command Port Base Address Register: Low Byte	
<7:0>	R/W	KBC Module Command Port Base Address: KBC_CMD_BA[7:0].	64h

### 6.3.2.3 KBC Interrupt Control Register

Below is the interrupt routing selection for encoding KBC interrupt in Serialized IRQ message. When the KBC\_Cfg\_70h<3:0> is programmed to 0000b or 1101b, or when the KBC function is disabled (KBC\_Cfg\_30h<0>=0), the KBC interrupt will not be encoded in SERIRQ message.

KBC_Cfg_70h		KBC Interrupt Control Register	
<7:4>	RO	Reserved	0000b
<3:0>	R/W	KBC Interrupt Routing Register to SERIRQ slot. 0000, 1101: No interrupt. 0001: IRQ1 slot.                      0010: SMI# slot. 0011-1100: IRQ3-IRQ12 slots.    1110-1111: IRQ14-IRQ15 slots.	0001b

### 6.3.2.4 KBC Interrupt Type Register

The access attribute of KBC\_Cfg\_71h<1:0> is **read only** (when KBC\_Cfg\_F0h<0>=0) or read-/write-able (when KBC\_Cfg\_F0h<0>=1).

The default KBC interrupt from the KBC module is active high and remains at high until an I/O read from KBC Data port is on to clear the KBC interrupt. For system makers, when the sharing of the KBC interrupt with the interrupt from other devices or other chip is intended, the KBC\_Cfg\_71h<1:0> should be programmed to 00b or 01b, depending on the system interrupt controller configuration.

KBC_Cfg_71h		KBC Interrupt Type Register	
<7:2 >	RO	Reserved	000000b
<1:0>	RO or R/W	KBC_Cfg_71h<1> is used to set the KBC Interrupt Level: 0: Active Low.                      1: Active High. KBC_Cfg_71h<0> is used to set the KBC Interrupt Trigger Type: 0: Edge Trigger.                      1: Level Trigger.  For example, KBC_IRQ behavior depends on KBC_Cfg_71h<1:0>: 00: Trigger low pulse for Edge-Trigger (IRQ sharing allowed). 01: Interrupt is inverted for Level-Trigger (IRQ sharing allowed). 1X: To IRQ routing directly for Edge-Trigger (IRQ cannot be shared).	10b

### 6.3.2.5 KBC Special Configuration Register

- KBC\_Cfg\_F0h<7> is used to enable Port\_92 FastGA20 and FastRST#. When enabled, the Port\_92h<1> is the FastGA20 control bit; and the Port\_92h<0> is the FastRST#. Whenever this Port\_92h<0> is programmed from 0 to 1, the IT8761E will issue a 6.6μs low pulse (on KBRST# signal) after 15μs. The Port\_92h<0> should be written as 0 before next FastRST# application. If the system chipset re-routes the KBRST# to software reset (INIT# to CPU), then the settings of the IT8761E still remains at the same configured value. If the system chipset re-routes the KBRST# to hardware reset (PCIRST#) and extend for more than 10μs (microseconds), then all the settings of the IT8761E will be reset to default values. However, if the system chipset re-route the KBRST# to hardware reset (PCIRST#) and without extending PCIRST# active low pulse ( $\leq 9\mu s$ ), then the KBC\_Cfg\_XXh will preserve the configured values, but other IT8761E PnP registers will still be reset to default values.
- KBC\_Cfg\_F0h<6> is used to select the KBC A20M# (AKA GA20) source. When cleared to 0, the KBC GA20 is generated from the output port bit 1 of 8042 μP; when set to 1, the KBC GA20 is generated from state machine emulated logic which emulates the data bit 1 written to KBC Data port of KBC D1h command.
- KBC\_Cfg\_F0h<5> is used to select the KBC RC (AKA KBC RST#) source. When cleared to 0, the KBC RST# is generated from the output port bit 0 of 8042 μP; when set to 1, the KBC RST# is generated from state machine emulated KBC FEh command. The IT8761E will issue a 6.6μs low pulse (on KBRST# signal) after 15μs.
- KBC\_Cfg\_F0h<4:3> is used to select the KBC operation frequency.
- KBC\_Cfg\_F0h<2> not only stops KBC operation clock, but is also used for Reset KBC operations. This bit is only for test in this version.
- KBC\_Cfg\_F0h<0> controls the write protection of KBC\_Cfg\_71h<1:0>.

KBC_Cfg_F0h		KBC Special Configuration Register	
<7>	R/W	Reserved	0b
<6>	R/W	Reserved	0b
<5>	R/W	Reserved	0b
<4:3>	R/W	KBC Clock: 00: 12 MHz.                      01: 8 MHz. 1X: 0 MHz (Stop KBC clock to power down).	00b
<2>	R/W	Reserved (KBC fully Power Down Control): 0: Normal operation. 1: Reset KBC module. At least 5ms is required to initialize the KBC module before accessing KBC after this bit is set from 1 to 0.	0b
<1>	R/W	Reserved	0b
<0>	R/W	Enable KBC Interrupt Type programming: 0: KBC_Cfg_71h<1:0> are read only. 1: KBC_Cfg_71h<1:0> are read/write.	0b

### 6.3.2.6 Emulated KBC Host Interface Control Register

This register is reserved for chip vendor to test a part of supported KBC commands. The enabling on the KBC\_Cfg\_F1h<7> may cause KBC  $\mu$ P r/w accessing failure.

After the KBC\_Cfg\_F1h<7> is enabled, some KBC commands may be intercepted by Emulated KBC Host Interface module (via programming the other bits of KBC\_Cfg\_F1h). That is, the 8042  $\mu$ P will not receive any KBC Status port reads and the current intercepted command until next un-intercepted KBC command. During the interception time, the Emulated KBC Host Interface module will respond to KBC status reads with immediately ready status (IBF=0; OBF=1 for AAh/D1h commands).

KBC_Cfg_F1h		Reserved (Emulated KBC Host Interface Control Register)	
<7>	R/W	Reserved (for testing KBC Host Interface: ) 0: 8042 Microprocessor, Normal operation. 1: State Machine Emulated Host interface. Both the PS/2 Keyboard and Mouse interface will be disabled.	0b
<6>	R/W	Reserved (for testing KBC Host Interface when KBC_Cfg_F1h<7>=1: ) 0: Bypass KBC AA command (Self-test). 1: Intercept KBC AA command by Emulated KBC Host Interface. (If the KBC 8042 $\mu$ P never receives a Self-Test command at least once, then the 8042 $\mu$ P may not accept other commands, and cause both KBC/Mouse devices operation failure.	1b
<5>	R/W	Reserved (for testing KBC Host Interface when KBC_Cfg_F1h<7>=1: ) 0: Bypass KBC D1 command (no GA20 & output port control). 1: Intercept KBC D1 command by Emulated KBC Host Interface. (The KBC_Cfg_F0<6> must also be set to 1.)	1b
<4>	R/W	Reserved (for testing KBC Host Interface when KBC_Cfg_F1h<7>=1: ) 0: Bypass KBC FE command (KBRST# control). 1: Intercept KBC FE command by Emulated KBC Host Interface. (The KBC_Cfg_F0<5> must also be set to 1.)	1b
<3:0>	R/W	Reserved	1111b



### 6.3.3 IT8761E UART PnP Registers (LDN=01h)

When the Global\_Cfg\_07h is programmed as 01h in the IT8761E configuration sequence, the UART device of the IT8761E is then selected. After the following PnP programming with index between 30h~FFh is applied to the UART device, either the Global\_Cfg\_07h value can then be changed or the IT8761E Configuration Sequence can exit.

UART_Cfg_30h		UART Function Enable Control Register	
<7:1>	RO	Reserved	0000000b
<0>	R/W	UART Function Enable Control. 0: Disable. 1: Enable.	0b

#### 6.3.3.1 UART Module Base Address Registers

The UART Module occupies 8-bytes I/O space. Its base address is programmed in UART\_Cfg\_60h and UART\_Cfg\_61h to form a 16-bits I/O address, with the default value at 03F8h.

UART_Cfg_60h		UART Module Base Address Pointer Register: High Byte	
<7:0>	R/W	UART Module Base Address Pointer: UART_BA[15:8].	03h

UART_Cfg_61h		UART Module Base Address Pointer Register: Low Byte	
<7:0>	R/W	UART Module Base Address Pointer: UART_BA[7:0]. The bits<2:0> are Read only as 000b.	F8h

#### 6.3.3.2 UART Interrupt Control Register

Below is the interrupt routing selection for encoding UART interrupts in Serialized IRQ message. When the UART\_Cfg\_70h<3:0> is programmed to 0000b or 1101b, or when the UART function is disabled (UART\_Cfg\_30h<0>=0), the UART interrupt will not be encoded in SERIRQ message.

UART_Cfg_70h		UART Interrupt Control Register	
<7:4 >	RO	Reserved	0000b
<3:0>	R/W	UART Interrupt Routing Register to SERIRQ slot. 0000, 1101: No interrupt. 0001: IRQ1 slot. 0010: SMI# slot. 0011-1100: IRQ3-IRQ12 slots. 1110-1111: IRQ14-IRQ15 slots.	0100b

### 6.3.3.3 UART Interrupt Type Register

The access attribute of UART\_Cfg\_71h<1:0> is **read only** (when UART\_Cfg\_F0h<0>=0) or read-/write-able (when UART\_Cfg\_F0h<0>=1).

The default UART interrupt from UART module is active high and it keeps at high until an I/O read from the UART IIR(and MSR) is on to clear UART interrupt. For system makers, if the sharing of the UART interrupt with the interrupt from other devices or other chip is intended, the UART\_Cfg\_71h<1:0> should be programmed to 00b or 01b, depending on system interrupt controller configuration.

UART_Cfg_71h		UART Interrupt Type Register	
<7:2 >	RO	Reserved	000000b
<1:0>	RO or R/W	UART_Cfg_71h<1> is used to set the UART Interrupt Level: 0: Active Low.                      1: Active High. UART_Cfg_71h<0> is used to set the UART Interrupt Trigger Type: 0: Edge Trigger.                  1: Level Trigger. For example, UART_IRQ behavior depends on Mouse_Cfg_71h<1:0>: 00: Trigger low pulse for Edge-Trigger (IRQ sharing allowed). 01: Interrupt is inverted for Level-Trigger (IRQ sharing allowed). 1X: To IRQ routing directly for Edge-Trigger (IRQ cannot be shared.).	10b

### 6.3.3.4 UART Special Configuration Register

- UART\_Cfg\_F0h<2:1> is left for chip testing or faster BAUD rate supports.
- UART\_Cfg\_F0h<0> controls the write protection of UART\_Cfg\_71h<1:0>.

UART_Cfg_F0h		UART Special Configuration Register	
<7:3>	RO	Reserved	00000b
<2:1>	R/W	UART Clock Source: 00: 24/13 MHz.    01: 48/13 MHz.    10: 48*2/13 MHz    11: 24 MHz.	00b
<0>	R/W	Enable UART Interrupt Type programming: 0: UART_Cfg_71h<1:0> are read only. 1: UART_Cfg_71h<1:0> are read/write.	0b

### 6.3.4 IT8761E GPIO PnP Registers (LDN=02h)

When the Global\_Cfg\_07h is programmed as 02h in the IT8761E configuration sequence, the GPIO device of the IT8761E is the selected. After the following PnP programming with index between 30h~FFh is applied to the GPIO device, either the Global\_Cfg\_07h value can then be changed or the IT8761E Configuration Sequence can be exited.

For system makers, if the GPIO function is intended, the RTS1# pin should be Pull/Up for Reset strap setting to select GPIO/FDC-related signals as GPIO interface. If the FDC function is intended, the RTS1# pin should be Pull/Down for Reset Strap setting to select GPIO/FDC-related signals as FDC interface. Those affected signals are GPIO2[7:0] and GPIO1[7:2].

The GPIO1[1:0] is multiplexed with PS/2 Mouse interface. If the Mouse function is disabled, the GPIO functions on GPIO1[1:0] still remains even when the FDC interface is selected.

#### 6.3.4.1 GPIO Module Base Address Registers

The GPIO Module occupies 4-byte I/O space. Its base address is programmed in GPIO\_Cfg\_60h and GPIO\_Cfg\_61h to form a 16-bit I/O address, with the default value at 0290h.

GPIO_Cfg_60h		GPIO Module Base Address Register: High Byte	
<7:0>	R/W	GPIO Base Address Pointer: GPIO_BA[15:8].	02h
GPIO_Cfg_61h		GPIO Module Base Address Register: Low Byte	
<7:0>	R/W	GPIO Base Address Pointer: GPIO_BA[7:0]. The bits<1:0> is read only as 00b.	90h

#### 6.3.4.2 GPIO Interrupt Control Register

Below is the interrupt routing selection for encoding GPIO interrupts in Serialized IRQ message. When the GPIO\_Cfg\_70h<3:0> is programmed to 0000b or 1101b, the GPIO interrupt (not including Software IRQ) will not be encoded in SERIRQ message.

GPIO_Cfg_70h		GPIO Interrupt Control Register	
<7:4>	RO	Reserved	0000b
<3:0>	R/W	GPIO Interrupt Routing Register to SERIRQ slot: 0000, 1101: No interrupt. 0001: IRQ1 slot.                      0010: SMI# slot. 0011-1100: IRQ3~IRQ12 slots.      1110-1111: IRQ14~IRQ15 slots.	0000b

### 6.3.4.3 GPIO Interrupt Type Register

The access attribute of GPIO\_Cfg\_71h<1:0> is **read only** (when GPIO\_Cfg\_FEh<0>=0) or read-/write-able (when GPIO\_Cfg\_FEh<0>=1).

The default GPIO interrupt from GPIO module is active high and it keeps at high until write-1-to-clear to GPIO\_Base+0002h and/or GPIO\_Bas+0003h to clear GPIO interrupts. For system makers, if the sharing of the GPIO interrupts with the interrupt from other devices or other chip is intended, the GPIO\_Cfg\_71h<1:0> should be programmed to 00b or 01b, depending on system interrupt controller configuration.

GPIO_Cfg_71h		GPIO Interrupt Type Register	
<7:2>	RO	Reserved	000000b
<1:0>	RO or R/W	GPIO_Cfg_71h<1> is used to set the GPIO Interrupt Level: 0: Active Low.                      1: Active High. GPIO_Cfg_71h<0> is used to set the GPIO Interrupt Trigger Type: 0: Edge Trigger.                1: Level Trigger. For example, GPIO_IRQ behavior depends on GPIO_Cfg_71h<1:0>: 00: Trigger low pulse for Edge-Trigger (IRQ sharing allowed). 01: Interrupt is inverted for Level-Trigger (IRQ sharing allowed). 1X: To IRQ routing directly for Edge-Trigger (IRQ cannot be shared.).	10b

### 6.3.4.4 GPIO Input / Output Selection Registers

Each GPIO pin can be programmed as GPIO input or GPIO output via controlling the Output-Enable of each GPIO bi-directional buffer.

- The GPIO1X Input / Output Selection Register controls the Output-Enable of GPIO1[n] bi-directional buffer. The output values are programmed in GPIO\_Base+0000h register.
- The GPIO2X Input / Output Selection Register controls the Output-Enable of GPIO2[n] bi-directional buffer. The output values are programmed in GPIO\_Base+0001h register.

GPIO_Cfg_F0h		GPIO1X Input / Output Selection Register	
<7:0>	R/W	GPIO1[7:0] Input / Output Selection. 0: Input.    1: Output.	F0h

GPIO_Cfg_F1h		GPIO2X Input / Output Selection Register	
<7:0>	R/W	GPIO2[7:0] Input / Output Selection. 0: Input.    1: Output.	FFh

### 6.3.4.5 GPIO Input Interrupt Mask Registers

For system Housekeeping routine to monitor the GPIO status, one method is to poll the GPIO\_Base+0000h or GPIO\_Base+0002h registers which reflect the GPIO signals' status; the other method is to service the interrupt from GPIO transition. Each GPIO pin can be programmed to generate GPIO interrupts or not. Once enabled and there exists a transition to trigger interrupts, the GPIO interrupt service routine will act to check the source GPIO\_Base+0002h and GPIO\_Base+0003h to identify which GPIO event has just occurred.

For those GPIO pins set in output direction, their interrupt mask bits must be set to 0 to avoid unexpected GPIO interrupts when controlling the GPIO outputs. When the FDC function is selected for the IT8761E, these bits in GPIO\_Cfg\_F2h<7:2> and GPIO\_Cfg\_F3h<7:0> should all be left at 0.

- The GPIO1X Input Interrupt Mask Register enables GPIO1[n] to be one source for GPIO interrupt generation. The GPIO1[7:6, 1:0] inputs are connected from GPIO17/GPIO16 and GPIO11/GPIO10 pins and the GPIO1[5:2] inputs are connected from De-Bouncing processed GPIO15~GPIO12 pins.
- The GPIO2X Input Interrupt Mask Register enables GPIO2[n] to be one source for GPIO interrupt generation. The GPIO2[7:0] inputs are connected from GPIO27~GPIO20 pins.

GPIO_Cfg_F2h		GPIO1X Input Interrupt Mask Register	
<7:0>	R/W	GPIO1[7:0] Input can still be reflected to Status, but may be masked for not generating interrupts. 0: Input is masked to interrupts.      1: Input is gated to GPIO Interrupts.	00h

GPIO_Cfg_F3h		GPIO2X Input Interrupt Mask Register	
<7:0>	R/W	GPIO2[7:0] Input can still be reflected to Status, but may be masked for not generating interrupts. 0: Input is masked to interrupts.      1: Input is gated to GPIO Interrupts.	00h

### 6.3.4.6 GPIO Interrupt Trigger Edge Registers

Each GPIO pin, when unmasked, can be programmed to generate GPIO interrupts on GPIOxx input rising or falling edge. If both rising/falling edges are required at the same time to generate GPIO interrupts for special purpose, then the system makers can assign two GPIO inputs for one external event signal.

- The GPIO1X Input Trigger Edge Register selects the active edge of GPIO1[n] to trigger GPIO interrupt.
- The GPIO2X Input Trigger Edge Register selects the active edge of GPIO2[n] to trigger GPIO interrupt.

GPIO_Cfg_F4h		GPIO1X Interrupt Trigger Edge Register	
<7:0>	R/W	Interrupt Trigger on which edge of GPIO1[7:0]: 0: Rising edge (Non-Inverting).      1: Falling edge (inverted).	00h

GPIO_Cfg_F5h		GPIO2X Interrupt Trigger Edge Register	
<7:0>	R/W	Interrupt Trigger on which edge of GPIO2[7:0]: 0: Rising edge (Non-Inverting).      1: Falling edge (inverted).	00h

### 6.3.4.7 GPIO De-bounce Register

The IT8761E supports four input de-bouncing filters for GPIO15~GPIO12 inputs. This is useful for connecting Push Button to GPIO input. If De-bouncing is disabled, then the GPIO1X will bypass de-bouncing logic and connect to GPIO module directly for instant GPIO status response.

GPIO_Cfg_F6h		GPIO De-bounce Register	
<7:6>	R/W	De-bounce on GPIO15 input: 00: Disable De-bouncing. 01: 10ms De-Bouncing. 10: 20ms De-bouncing. 11: 40ms De-Bouncing.	00b
<5:4>	R/W	De-bounce on GPIO14 input: 00: Disable De-bouncing. 01: 10ms De-Bouncing. 10: 20ms De-bouncing. 11: 40ms De-Bouncing.	00b
<3:2>	R/W	De-bounce on GPIO13 input: 00: Disable De-bouncing. 01: 10ms De-Bouncing. 10: 20ms De-bouncing. 11: 40ms De-Bouncing.	00b
<1:0>	R/W	De-bounce on GPIO12 input: 00: Disable De-bouncing. 01: 10ms De-Bouncing. 10: 20ms De-bouncing. 11: 40ms De-Bouncing.	00b

### 6.3.4.8 GPIO Blinking Register

The IT8761E supports two independent blinking controls on GPIO21 and GPIO20. The blinking function is normally used as LED driving for human interface to show different system operating modes or power down levels. The method is to program the GPIO21 (or GPIO20) as GPIO output direction (in GPIO\_Cfg\_F1h) with its GPIO output value set to 0 (in GPIO\_Base+0001h). If the blinking function is enabled (the value of GPIO\_Cfg\_F7h<3:2> or GPIO\_Cfg\_F7h<1:0> is not 00b), then the IT8761E will drive GPIO21 (or GPIO20) signal as a square wave with programmable duty cycles. If the blinking is disabled (the value of GPIO\_Cfg\_F7h<3:2> or GPIO\_Cfg\_F7h<1:0> is 00b), then the GPIO21 (or GPIO20) works just as the other normal GPIO function and reflects the output value (programmed in GPIO\_Base+0001h) directly to external signal pin.

GPIO_Cfg_F7h		GPIO Blinking Register	
<7:4>	RO	Reserved	0000b
<3:2>	R/W	GPIO21 Blinking when Output Value (GPIO_Base+0001h<1>) is 0: 00: Just output 0 (always bright). 01: High 0.70sec, Low 0.70sec (bright with 1/2 duty cycle). 10: High 1.05sec, Low 0.35sec (bright with 1/4 duty cycle). 11: High 2.45sec, Low 0.35sec (bright with 1/8 duty cycle).	00b
<1:0>	R/W	GPIO20 Blinking when Output Value (GPIO_Base+0001h<0>) is 0: 00: Just output 0 (always bright). 01: High 0.70sec, Low 0.70sec (bright with 1/2 duty cycle). 10: High 1.05sec, Low 0.35sec (bright with 1/4 duty cycle). 11: High 2.45sec, Low 0.35sec (bright with 1/8 duty cycle).	00b

### 6.3.4.9 Software Interrupt Registers

The IT8761E provides software programmable interrupt generator for special system purpose. There are 16 independent interrupt trigger sources, and will be encoded to Serialized IRQ message in IRQ[0:1, 3:12, 14:15], SMI# and IOCHCK# frames. Each encoding comes with an enable bit and a trigger bit. When a S/W interrupt is enabled, writing a 1 to its trigger bit will cause the IT8761E to generate a 30ns (one PCICLK period) low pulse in relative SERIRQ coding frame for only 1 SERIRQ message, and tri-state in other SERIRQ message. The trigger bit is self-cleared. Writing a 0 to the trigger bit will not have any effects.

- The enable bits for 16 S/W interrupts are programmed in GPIO\_Cfg\_F8h or GPIO\_Cfg\_F9h, with the default value at 00h, all disabled.
- The trigger bits for 16 S/W interrupts are programmed in GPIO\_Cfg\_FAh or GPIO\_Cfg\_FBh. Reading these registers always gets 00h.

GPIO_Cfg_F8h		Software Interrupt Trigger Enable Register - 1	
<7>	R/W	Enable Software Interrupt Trigger in IRQ7 frame of SERIRQ: 0: Disable    1: Enable IRQ7 Trigger if GPIO_Cfg_FAh<7> is set to 1.	0b
<6>	R/W	Enable Software Interrupt Trigger in IRQ6 frame of SERIRQ: 0: Disable    1: Enable IRQ6 Trigger if GPIO_Cfg_FAh<6> is set to 1.	0b
<5>	R/W	Enable Software Interrupt Trigger in IRQ5 frame of SERIRQ: 0: Disable    1: Enable IRQ5 Trigger if GPIO_Cfg_FAh<5> is set to 1.	0b
<4>	R/W	Enable Software Interrupt Trigger in IRQ4 frame of SERIRQ: 0: Disable    1: Enable IRQ4 Trigger if GPIO_Cfg_FAh<4> is set to 1.	0b
<3>	R/W	Enable Software Interrupt Trigger in IRQ3 frame of SERIRQ: 0: Disable    1: Enable IRQ3 Trigger if GPIO_Cfg_FAh<3> is set to 1.	0b
<2>	R/W	Enable Software Interrupt Trigger in SMI# frame of SERIRQ: 0: Disable    1: Enable SMI# Trigger if GPIO_Cfg_FAh<2> is set to 1.	0b
<1>	R/W	Enable Software Interrupt Trigger in IRQ1 frame of SERIRQ: 0: Disable    1: Enable IRQ1 Trigger if GPIO_Cfg_FAh<1> is set to 1.	0b
<0>	R/W	Enable Software Interrupt Trigger in IRQ0 frame of SERIRQ: 0: Disable    1: Enable IRQ0 Trigger if GPIO_Cfg_FAh<0> is set to 1.	0b

GPIO_Cfg_F9h		Software Interrupt Trigger Enable Register - 2	
<7>	R/W	Enable Software Interrupt Trigger in IRQ15 frame of SERIRQ: 0: Disable 1: Enable IRQ15 Trigger if GPIO_Cfg_FBh<7> is set to 1.	0b
<6>	R/W	Enable Software Interrupt Trigger in IRQ14 frame of SERIRQ: 0: Disable 1: Enable IRQ14 Trigger if GPIO_Cfg_FBh<6> is set to 1.	0b
<5>	R/W	Enable Software Interrupt Trigger in IOCHK# frame of SERIRQ: 0: Disable 1: Enable IOCHK# Trigger if GPIO_Cfg_FBh<5> is set to 1.	0b
<4>	R/W	Enable Software Interrupt Trigger in IRQ12 frame of SERIRQ: 0: Disable 1: Enable IRQ12 Trigger if GPIO_Cfg_FBh<4> is set to 1.	0b
<3>	R/W	Enable Software Interrupt Trigger in IRQ11 frame of SERIRQ: 0: Disable 1: Enable IRQ11 Trigger if GPIO_Cfg_FBh<3> is set to 1.	0b
<2>	R/W	Enable Software Interrupt Trigger in IRQ10 frame of SERIRQ: 0: Disable 1: Enable IRQ10 Trigger if GPIO_Cfg_FBh<2> is set to 1.	0b
<1>	R/W	Enable Software Interrupt Trigger in IRQ9 frame of SERIRQ: 0: Disable 1: Enable IRQ9 Trigger if GPIO_Cfg_FBh<1> is set to 1.	0b
<0>	R/W	Enable Software Interrupt Trigger in IRQ8 frame of SERIRQ: 0: Disable 1: Enable IRQ8 Trigger if GPIO_Cfg_FBh<0> is set to 1.	0b

GPIO_Cfg_FAh		Software Interrupt Trigger Register - 1	
<7>	R/W	Software Set to 1 will drive IRQ7 low for one SERIRQ message period. This bit is self-cleared and always read as 0.	0b
<6>	R/W	Software Set to 1 will drive IRQ6 low for one SERIRQ message period. This bit is self-cleared and always read as 0.	0b
<5>	R/W	Software Set to 1 will drive IRQ5 low for one SERIRQ message period. This bit is self-cleared and always read as 0.	0b
<4>	R/W	Software Set to 1 will drive IRQ4 low for one SERIRQ message period. This bit is self-cleared and always read as 0.	0b
<3>	R/W	Software Set to 1 will drive IRQ3 low for one SERIRQ message period. This bit is self-cleared and always read as 0.	0b
<2>	R/W	Software Set to 1 will drive SMI# low for one SERIRQ message period. This bit is self-cleared and always read as 0.	0b
<1>	R/W	Software Set to 1 will drive IRQ1 low for one SERIRQ message period. This bit is self-cleared and always read as 0.	0b
<0>	R/W	Software Set to 1 will drive IRQ0 low for one SERIRQ message period. This bit is self-cleared and always read as 0.	0b



GPIO_Cfg_FBh		Software Interrupt Trigger Register - 2	
<7>	R/W	Software Set to 1 will drive IRQ15 low for one SERIRQ message period. This bit is self-cleared and always read as 0.	0b
<6>	R/W	Software Set to 1 will drive IRQ14 low for one SERIRQ message period. This bit is self-cleared and always read as 0.	0b
<5>	R/W	Software Set to 1 will drive IOCHK# low for one SERIRQ message period. This bit is self-cleared and always read as 0. (not IRQ13)	0b
<4>	R/W	Software Set to 1 will drive IRQ12 low for one SERIRQ message period. This bit is self-cleared and always read as 0.	0b
<3>	R/W	Software Set to 1 will drive IRQ11 low for one SERIRQ message period. This bit is self-cleared and always read as 0.	0b
<2>	R/W	Software Set to 1 will drive IRQ10 low for one SERIRQ message period. This bit is self-cleared and always read as 0.	0b
<1>	R/W	Software Set to 1 will drive IRQ9 low for one SERIRQ message period. This bit is self-cleared and always read as 0.	0b
<0>	R/W	Software Set to 1 will drive IRQ8 low for one SERIRQ message period. This bit is self-cleared and always read as 0.	0b

#### 6.3.4.10 GPIO Special Configuration Register

- GPIO\_Cfg\_FEh<0> controls the write protection of GPIO\_Cfg\_71h<1:0>.

GPIO_Cfg_FEh		GPIO Special Configuration Register	
<7:1 >	RO	Reserved	0000000b
<0>	R/W	Enable GPIO Interrupt Type programming: 0: GPIO_Cfg_71h<1:0> are read only. 1: GPIO_Cfg_71h<1:0> are read/write.	0b

### 6.3.5 IT8761E FDC PnP Registers (LDN=03h)

When the Global\_Cfg\_07h is programmed as 03h in the IT8761E configuration sequence, the FDC device of the IT8761E is then selected. After the following PnP programming with index between 30h~FFh is applied to FDC device, either the Global\_Cfg\_07h value can then be changed or the IT8761E Configuration Sequence can be exited.

#### 6.3.5.1 FDC Function Enable Control Register

The FDC\_Cfg\_30h<0> controls the enable/disable state of the IT8761E FDC function. For system makers, if the GPIO function is intended, then the RTS1# pin should be Pull/Up for Reset strap setting to select GPIO/FDC- related signals as GPIO interface. If the FDC function is intended, then the RTS1# pin should be Pull/Down for Reset Strap setting to select GPIO/FDC-related signals as FDC interface.

FDC_Cfg_30h		FDC Function Enable Control Register	
<7:1>	RO	Reserved	0000000b
<0>	R/W	FDC Function Enable Control: 0: Disable. 1: Enabled. But the default pin function and driving/direction control still depends on Reset-Strap value of RTS1# (Pin # 41).	0b

#### 6.3.5.2 FDC Module Base Address Registers

The FDC Module occupies 8-byte I/O space. Its base address is programmed in FDC\_Cfg\_60h and FDC\_Cfg\_61h to form a 16-bit I/O address, with the default value at 03F0h.

FDC_Cfg_60h		FDC Module Base Address Pointer Register: High Byte	
<7:0>	R/W	FDC Module Base Address Pointer: FDC_BA[15:8].	03h

FDC_Cfg_61h		FDC Module Base Address Pointer Register: Low Byte	
<7:0>	R/W	FDC Module Base Address Pointer: FDC_BA[7:0]. The bits<2:0> are Read only as 000b.	F0h

#### 6.3.5.3 FDC Interrupt Control Register

Below is the interrupt routing selection for encoding FDC interrupts in Serialized IRQ message. When the FDC\_Cfg\_70h<3:0> is programmed to 0000b or 1101b, or when the FDC function is disabled (FDC\_Cfg\_30h<0>=0), the FDC interrupts will not be encoded in SERIRQ message.

FDC_Cfg_70h		FDC Interrupt Control Register	
<7:4 >	RO	Reserved	0000b
<3:0>	R/W	FDC Interrupt Routing Register to SERIRQ slot: 0000, 1101: No interrupt. 0001: IRQ1 slot.                      0010: SMI# slot. 0011-1100: IRQ3-IRQ12 slots.      1110-1111: IRQ14-IRQ15 slots.	0110b

### 6.3.5.4 FDC Interrupt Type Register

The access attribute of FDC\_Cfg\_71h<1:0> is **read only** (when FDC\_Cfg\_FEh<0>=0) or read-/write-able (when FDC\_Cfg\_FEh<0>=1).

The default FDC interrupts from the FDC module is active high and it keeps at high until an appropriate FDC access is on to clear the FDC interrupts. For system makers, if the sharing of the FDC interrupt with the interrupt from other devices or other chip is intended, the FDC\_Cfg\_71h<1:0> should be programmed to 00b or 01b, depending on system interrupt controller configuration.

FDC_Cfg_71h		FDC Interrupt Type Register	
<7:2 >	RO	Reserved	000000b
<1:0>	RO or R/W	FDC_Cfg_71h<1> is for setting FDC Interrupt Level: 0: Active Low.                      1: Active High. FDC_Cfg_71h<0> is for setting FDC Interrupt Trigger Type: 0: Edge Trigger.                  1: Level Trigger. For example, FDC_IRQ behavior depends on Mouse_Cfg_71h<1:0>: 00: Trigger low pulse for Edge-Trigger (IRQ sharing allowed). 01: Interrupt is inverted for Level-Trigger (IRQ sharing allowed). 1X: To IRQ routing directly for Edge-Trigger (IRQ cannot be shared).	10b

### 6.3.5.5 FDC DMA Channel Register

The FDC DMA uses an 8-bit DMA channel, so the programmable DMA channel selection is limited in DMA Channel\_0 to Channel\_3, with the default at DMA Channel\_2. The LPC interface of the IT8761E will depend on this setting in coding FDC DMA request in LPC DMA request signal (LDRQ#, shared with GPIO12) and re-direct DACK2# (decoded in LPC LAD[3:0] message) to the FDC module.

FDC_Cfg_74h		FDC DMA Channel Register	
<7:3 >	RO	Reserved	00000b
<2:0>	R/W	DMA Channel Select (DREQn/DACKn#): 000: Channel_0.      001: Channel_1.      010: Channel_2. 011: Channel_3.      100: No DMA.          Others: Invalid.	010b

### 6.3.5.6 FDC Special Configuration Register – 1

- All the bits of FDC\_Cfg\_F0h<7:1> are reserved and should be kept at 0000110b for correct operation with current Floppy Disk Drives.
- FDC\_Cfg\_F0h<0> provides an alternate FDD write protect option. By setting to 1, the FDD will be limited as **read only** for special system network or security control.

FDC_Cfg_F0h		FDC Special Configuration Register - 1	
<7:6>	R/W	Reserved (FDC Drive Type Select[1:0]).	00b
<5:4>	R/W	Reserved (FDC Data Rate Table Select[1:0]).	00b
<3:2>	R/W	Reserved (for testing only) IDENT, MFM Control: 1X: PC/AT Mode. 00: PS/2 model 3-Mode.                      01: PS/2 models 50/60/80 Mode.	11b
<1>	R/W	Reserved (for testing only) FDC 3-Mode Enable: 0: PC/AT Normal Mode.                      1: Enable 3-Mode Floppy Support.	0b
<0>	R/W	Software Write Protect: 0: Normal Operation.                      1: Write Protect.	0b

### 6.3.5.7 FDC Special Configuration Register - 2

- FDC\_Cfg\_FEh<0> controls the write protection of FDC\_Cfg\_71h<1:0>.

FDC_Cfg_FEh		FDC Special Configuration Register - 2	
<7:1 >	RO	Reserved	0000000b
<0>	R/W	Enable FDC Interrupt Type programming: 0: FDC_Cfg_71h<1:0> are read only. 1: FDC_Cfg_71h<1:0> are read/write.	0b

### 6.3.6 IT8761E Mouse PnP Registers (LDN=04h)

When the Global\_Cfg\_07h is programmed as 04h in the IT8761E configuration sequence, the Mouse device of the IT8761E is then selected. After the following PnP programming with index between 30h~FFh is applied to Mouse device, either the Global\_Cfg\_07h value can then be changed or the IT8761E Configuration Sequence can be exited.

#### 6.3.6.1 Mouse Function Enable Control Register

The Mouse\_Cfg\_30h<0> controls the enable/disable state of the IT8761E Mouse function. The Mouse interface, MSCLK /MSDAT, is multiplexed with GPIO1[1:0].

Mouse_Cfg_30h		Mouse Function Enable Control Register	
<7:1>	RO	Reserved	0000000b
<0>	R/W	Mouse Function Enable Control. (KBC_Cfg_30h<0> needs to be enabled at first): 0: Disable, Pin#_17/15 are selected as GPIO1[1:0]. 1: Enable, Pin#_17/15 are selected as MSCLK/MSDAT.	0b

#### 6.3.6.2 Mouse Interrupt Control Register

Below is the interrupt routing selection for encoding Mouse interrupt in Serialized IRQ message. When the Mouse\_Cfg\_70h<3:0> is programmed to 0000b or 1101b, or when the Mouse function is disabled (Mouse\_Cfg\_30h<0>=0), the Mouse interrupt will not be encoded in SERIRQ message.

Mouse_Cfg_70h		Mouse Interrupt Control Register	
<7:4 >	RO	Reserved	0000b
<3:0>	R/W	Mouse Interrupt Routing Register to SERIRQ slot: 0000, 1101: No interrupt. 0001: IRQ1 slot.                      0010: SMI# slot. 0011-1100: IRQ3-IRQ12 slots.      1110-1111: IRQ14-IRQ15 slots.	1100b

Mouse_Cfg_F0h		Mouse Special Configuration Register	
<7:1 >	RO	Reserved	0000000b
<0>	R/W	Enable Mouse Interrupt Type programming: 0: Mouse_Cfg_71h<1:0> are read only. 1: Mouse_Cfg_71h<1:0> are read/write.	0b

#### 6.4 GPIO Functional Registers Description

GPIO_Base+0000h		GPIO1X Data/Status Register	
<7:0>	W	Output Data to be written to GPIO1[7:0]. For each bit (if its direction in GPIO_Cfg_F0h is output): 0: Output Low. 1: Output High.	F0h
<7:0>	R	Current GPIO1[7:0] pins value. For each bit read (after de-bounce process): 0: External GPIO1[n] is Low. 1: External GPIO1[n] is High.	NA

GPIO_Base+0001h		GPIO2X Data/Status Register	
<7:0>	W	Output Data to be written to GPIO2[7:0]. For each bit (if its direction in GPIO_Cfg_F1h is output): 0: Output Low. 1: Output High.	00h
<7:0>	R	Current GPIO2[7:0] pin values. For each bit read (for GPIO2[1:0], if selected as PS/2 Mouse interface, then always read as 00b): 0: External GPIO2[n] is Low. 1: External GPIO2[n] is High.	NA

GPIO_Base+0002h		GPIO1X Interrupt Source Register	
<7:0>	R/W1TC <sup>1</sup>	GPIO interrupt source from which pins of GPIO1[7:0]. For each bit, read 1 means the GPIO1[n] is one source to cause the GPIO interrupt; and only a write of 1 can clear this equivalent bit. Since there maybe multiple GPIO events to trigger the interrupt; thus, the driver reads this register and re-writes the value to de-assert the interrupt trigger events.	00h

GPIO_Base+0003h		GPIO2X Interrupt Source Register	
<7:0>	R/W1TC	GPIO interrupt source from which pins of GPIO2[7:0]. For each bit, read 1 means the GPIO2[n] is one source to cause the GPIO interrupt; and only a write of 1 can clear this equivalent bit. Since there maybe multiple GPIO events to trigger the interrupt; thus, the driver reads this register and re-writes the value to de-assert the interrupt trigger events.	00h

<sup>1</sup> W1TC: Write 1 to Clear status bit

## 7. Characteristics

### Absolute Maximum Ratings\*

Applied Voltage ( $V_{CC}$ ) ..... -0.3V to 6.0V

Input Voltage ( $V_I$ )..... -0.3V to  $V_{CC}+0.3V$

Output Voltage ( $V_O$ )..... -0.3V to  $V_{CC}+0.3V$

Storage Temperature ( $T_{STG}$ ) .... -40°C to 125°C

### \*Comments

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in “Recommended Operating Conditions” is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 7-1. Recommended Operating Conditions**

Symbol	Parameter	Min.	Typical	Max.	Unit
VCC	Power Supply	4.75	5.0	5.25	V
V33	Power Supply	3.0	3.3	3.6	V
$V_{IN}$	Input Voltage	0		VCC	V
$T_{OPT}$	Operating Temperature	0	25	70	°C

## 7.1 DC Electrical Characteristics

**Table 7-2. General DC Characteristics**

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
$I_{IL}$	Input Low Current	no P/D or P/U	-1		1	μA
$I_{IH}$	Input High Current	no P/D or P/U	-1		1	μA
$I_{OZ}$	Tri-state Leakage Current		-10		10	μA
$I_{CC}$	Operating Current	from VCC source				mA
$C_{IN}$	Input Capacitance			4		pF
$C_{OUT}$	Output Capacitance			4 to 6		pF
$C_{BID}$	Bi-directional Buffer Capacitance			4 to 6		pF



**Table 7-3. DC Electrical Characteristics for 5V Interface**  
( $T_{OPT}=0^{\circ}C\sim70^{\circ}C$ ,  $V_{CC}=4.75V\sim5.25V$ )

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
$V_{IL}$	Input Low Voltage	TTL			0.8	V
$V_{IL}$	Schmitt Input Low Voltage	TTL		1.10		V
$V_{IH}$	Input High Voltage	TTL	2.2			V
$V_{IH}$	Schmitt Input High Voltage	TTL		1.87		V
$V_{OL}$	Output Low Voltage	$I_{OL}=8, 16, 24mA$			0.4	V
$V_{OH}$	Output High Voltage	$I_{OH}=8, 16, 24mA$	3.5			V
$R_I$	Input P/U or P/D Resistance	$V_{IL}=0V$ , $V_{IH}=V_{CC}$				V

**Table 7-4. DC Electrical Characteristics for 3.3V Interface**  
( $T_{OPT}=0^{\circ}C\sim70^{\circ}C$ ,  $V_{33}=3.0V\sim3.6V$ )

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
$V_{IL}$	Input Low Voltage	COMS			$0.3 \cdot V_{33}$	V
$V_{IH}$	Input High Voltage	COMS	$0.7 \cdot V_{33}$			V
$V_{OL}$	Output Low Voltage	$I_{OL}=5mA$			0.4	V
$V_{OH}$	Output High Voltage	$I_{OH}=5mA$	2.3			V

## 7.2 AC Characteristics

**Table 7-5. AC Characteristics**  
(VCC=5.0V±5%, V33=3.3V±5%, Ta=0°C~70°C, CL=87pF) unit: ns

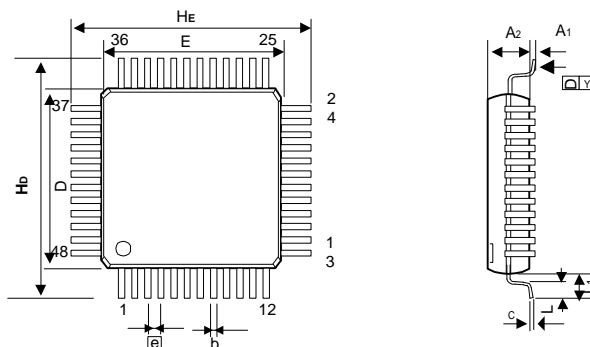
Symbol	Parameter	Min.	Typical	Max.	Notes
<b>Clock Input Timing</b>					
t <sub>CYC_CLK48</sub>	CLK48 Period		20.833		48.00 MHz
t <sub>Duty_CLK48</sub>	CLK48 High/Low time	9			
t <sub>CYC_LCLK</sub>	LCLK Period	30			As PCI Spec., 33 MHz
t <sub>Duty_LCLK</sub>	LCLK High/Low time	11			As PCI Spec.
<b>LPC Interface Timing</b>					
t <sub>ON_LPC</sub>	Float to Active time	2			
t <sub>OFF_LPC</sub>	Active to Float Delay time			28	
t <sub>VALID_LPC</sub>	Valid Output Delay time	2		20	
t <sub>SETUP_LPC</sub>	Input Setup time	7			
t <sub>HOLD_LPC</sub>	Input Hold time	2			

### 7.3 Waveform

## 8. Package Information

### 48 Pin LQFP Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A <sub>1</sub>	0.002	-	0.006	0.05	-	0.15
A <sub>2</sub>	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.008	0.011	0.17	0.20	0.27
c	0.004	-	0.008	0.09	-	0.20
D	0.274	0.276	0.278	6.95	7.00	7.05
E	0.274	0.276	0.278	6.95	7.00	7.05
e	0.02BSC			0.50BSC		
H <sub>D</sub>	0.350	0.354	0.358	8.90	9.00	9.10
H <sub>E</sub>	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L <sub>1</sub>	0.039REF			1.00REF		
y	-	-	0.004	-	-	0.10
θ	0°	-	7°	0°	-	7°

#### Notes:

- Dimensions D and E do not include mold protrusion.
- Dimensions b does not include dambar protrusion.  
Total in excess of the b dimension at maximum material condition.  
Dambar cannot be located on the lower radius of the foot.

**9. Ordering Information**

Part No.	Package
IT8761E	48 LQFP